IEEE ICMA 2006 Tutorial Workshop:

– Iterative Learning Control –
Algebraic Analysis and Optimal Design

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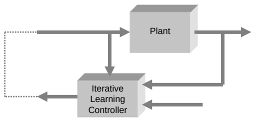

Acknowledgments

- My ex-colleagues, friends, co-inventors in Seagate Singapore Science Park Design Center. In particular,
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  - LinCheng Xiu, Qiang Bi, Jianbo He, Tao Zhang, and Xiong Liu
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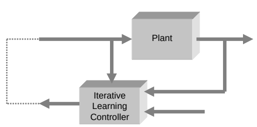
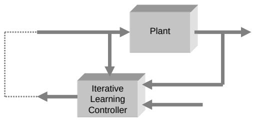
  - Kevin Gomez, ChoonKiat Ling and Beng Wee Quak.
- Seagate (US sites) ex-colleagues. In particular,
  - John Morris
  - Hai T. Ho
  - Gabor.G. Szita



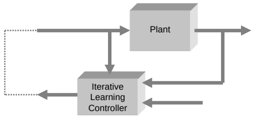
Outline

- – Some Background Information on HDDs
- – High TPI HDD Servo: Challenges and Limits.
- – The Story of Seagate U6
- – My Patents at Seagate
- – Why ILC in HDD
- – The Parsimonious Scheme
- – Drive level results
- – Concluding Remarks

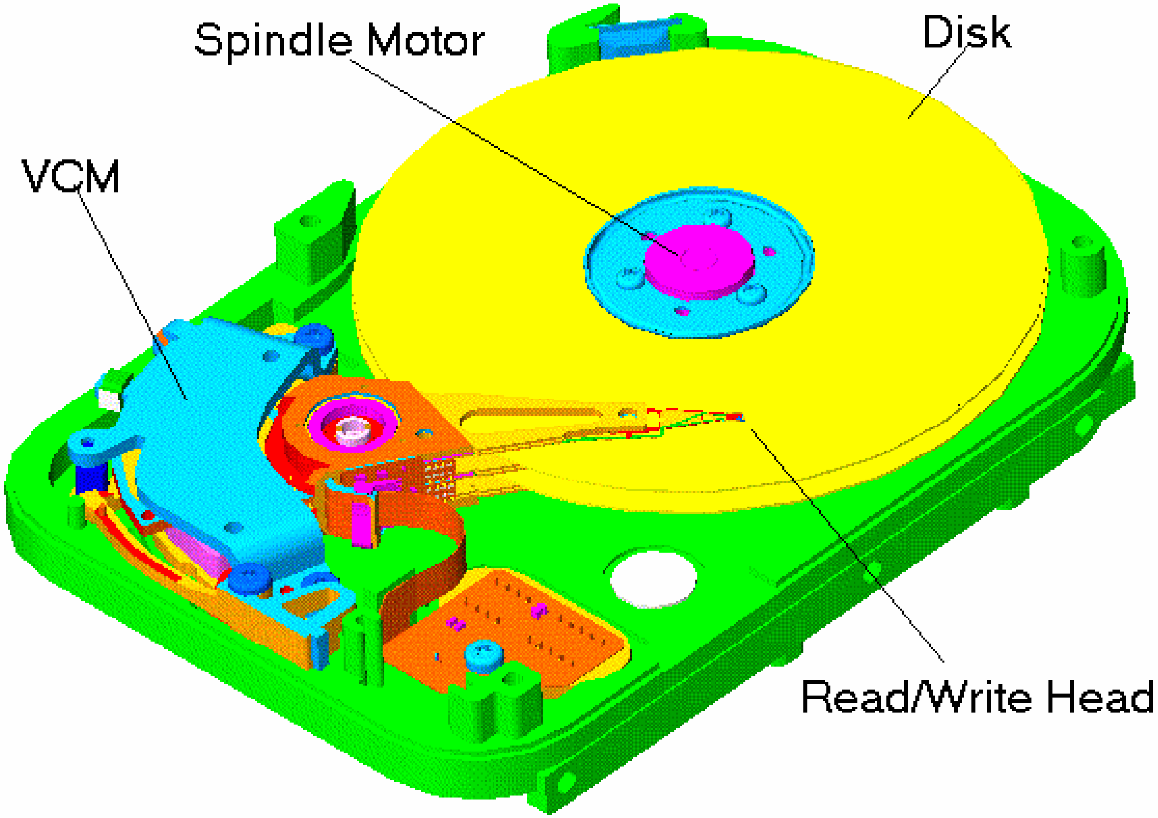


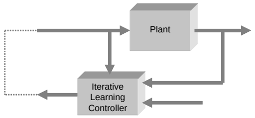
Hard Disk Drives (HDDs)

- Amazing mechatronic devices. Just plug-in and it will work reliably for years.
- First HDD introduced by IBM in 1957.
- Recording density increased by a factor of 10 million.
- In 1997, over 200 million HDDs produced with an average cost < $US 0.05/Mb.
- In 1999, total shipped HDD capacity: > 1 million Tb (10^{18})
- ...
- Need an enhanced appreciation of HDDs
  - W. Messner and R. Ehrlich. "*A Tutorial on Controls for Disk Drives*". **Proc. of the American Control Conference**, Arlington, VA, June 2001, pp.408-420

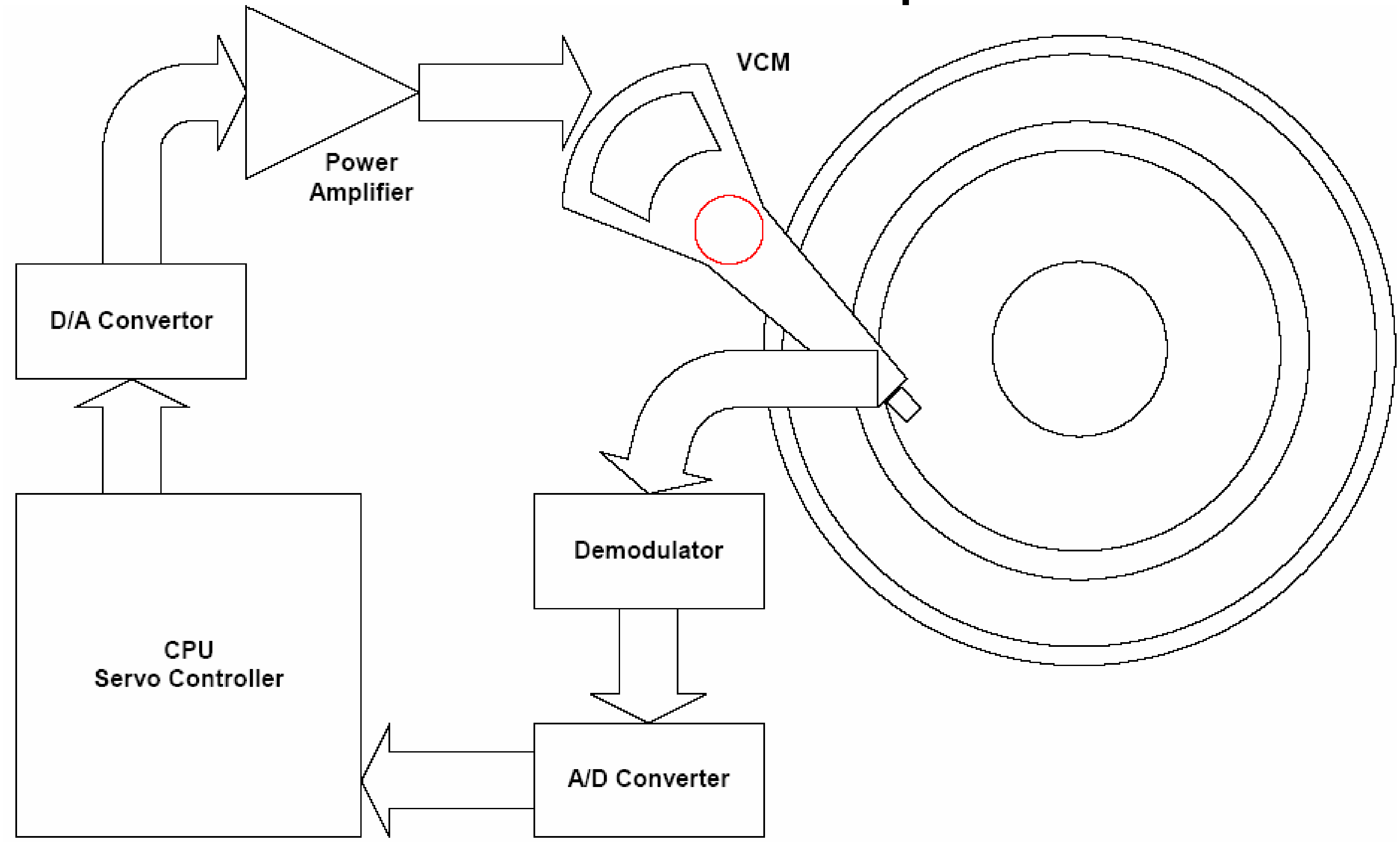


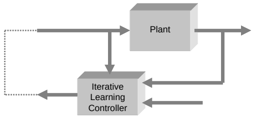
A Typical Hard Disk Drive (HDD)



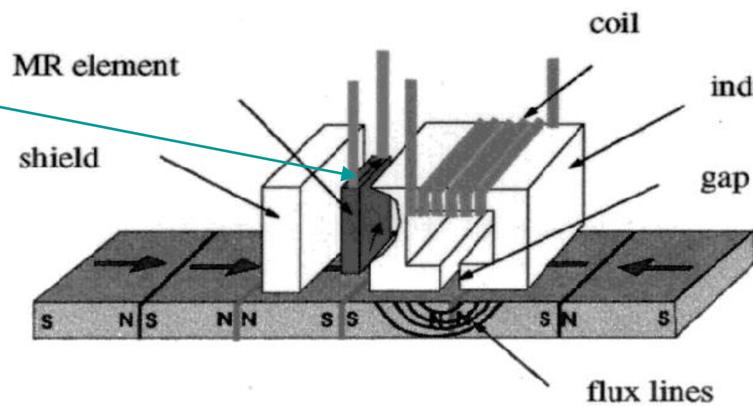


HDD Servo Loop





Magnetoresistive (MR) head (its resistance change due to magnetic field change)



Schematic of read/write transducer. (Source: Tom Albrecht, IBM)

Typical slider thickness: 0.5 mm.

Typical fly height: 20 nm
Think about a Boeing 747 flying at an altitude of a few mm.

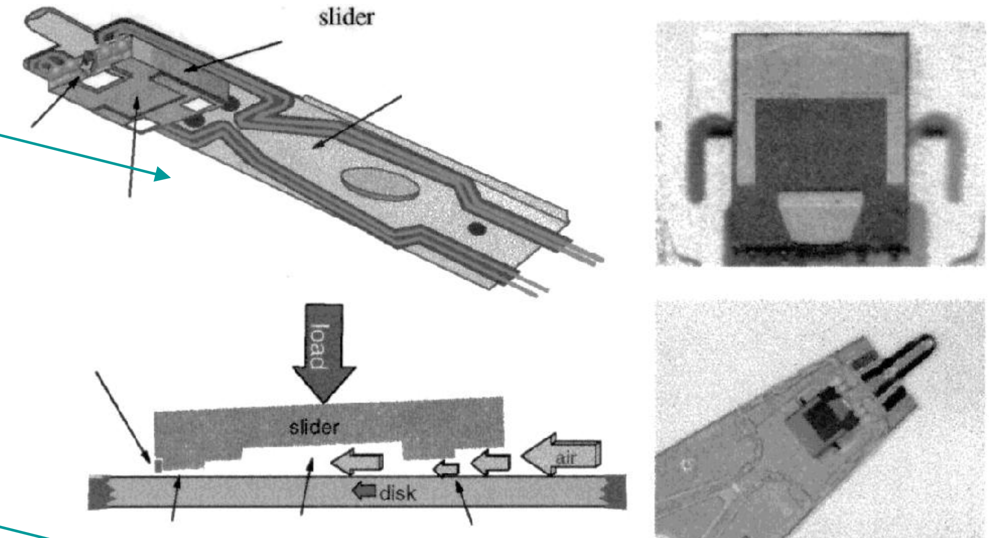
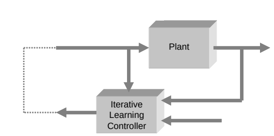
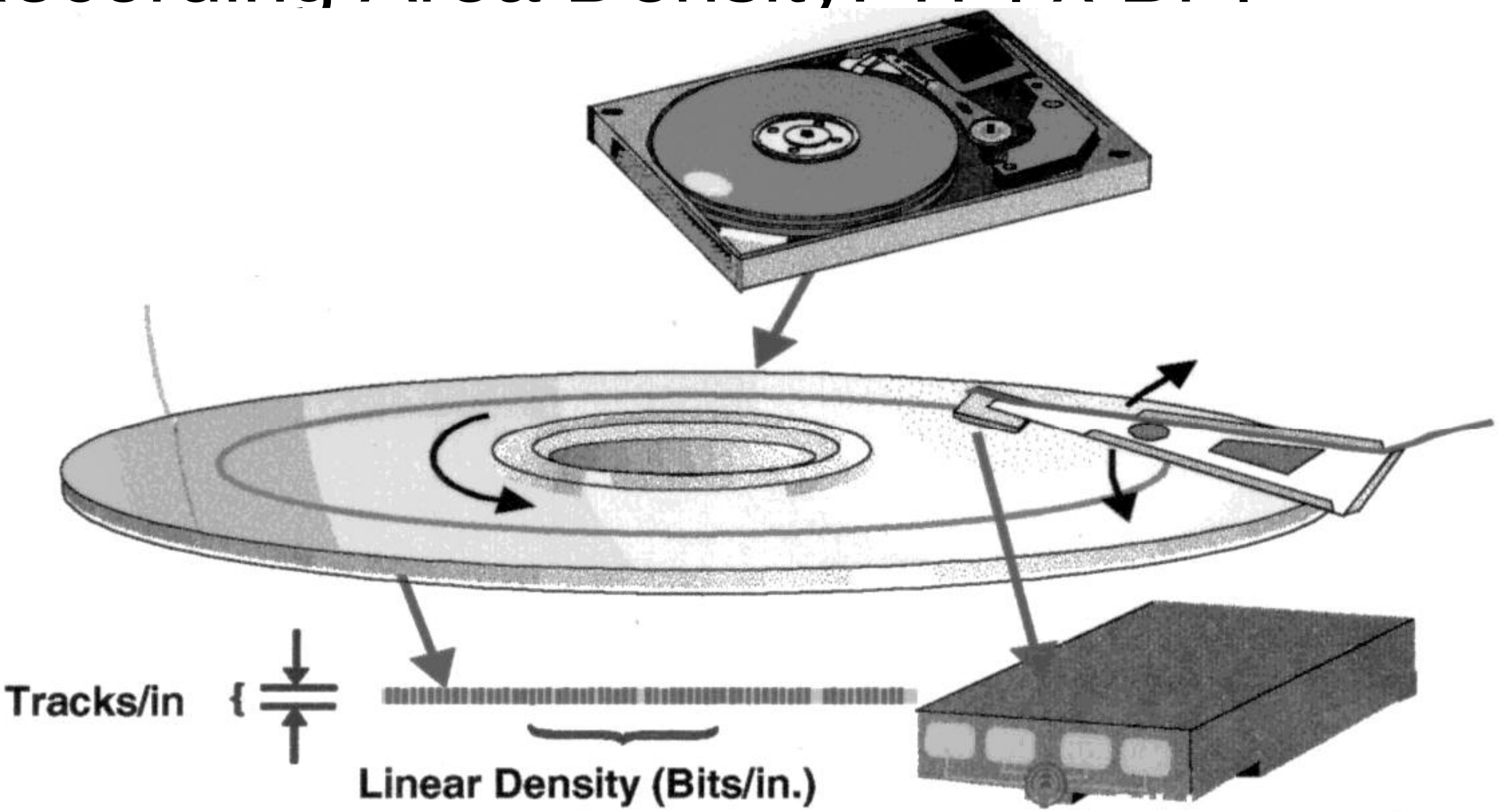


Illustration of suspension and slider. Left: schematic. Right: photograph. (Source: Tom Albrecht, IBM)

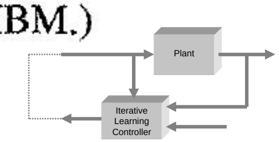
R/W Heads



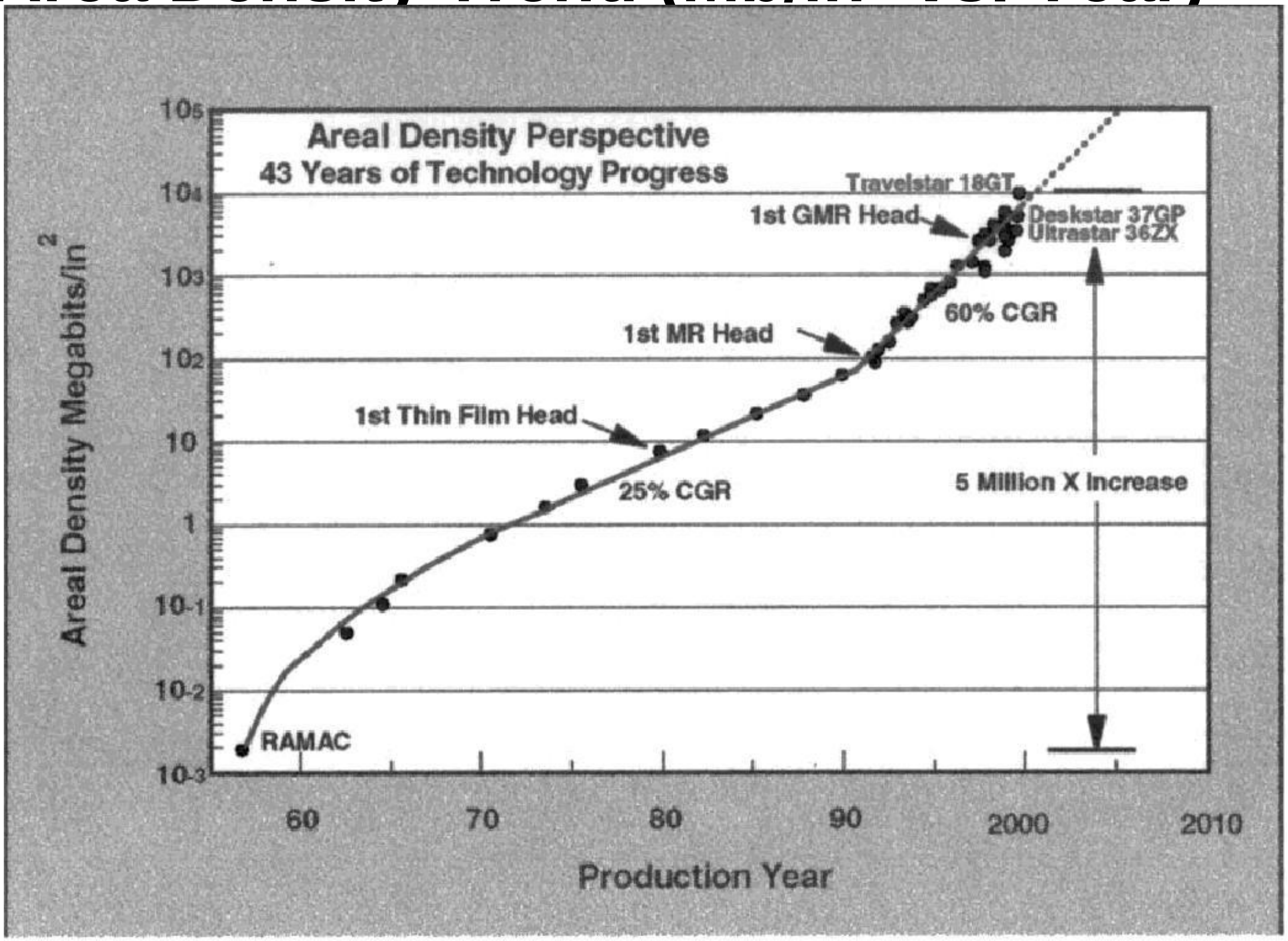
Recording Area Density: TPI x BPI



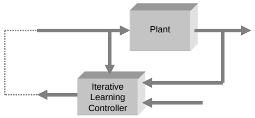
Schematic of important disk drive components. (Source: Tom Albrecht, IBM.)



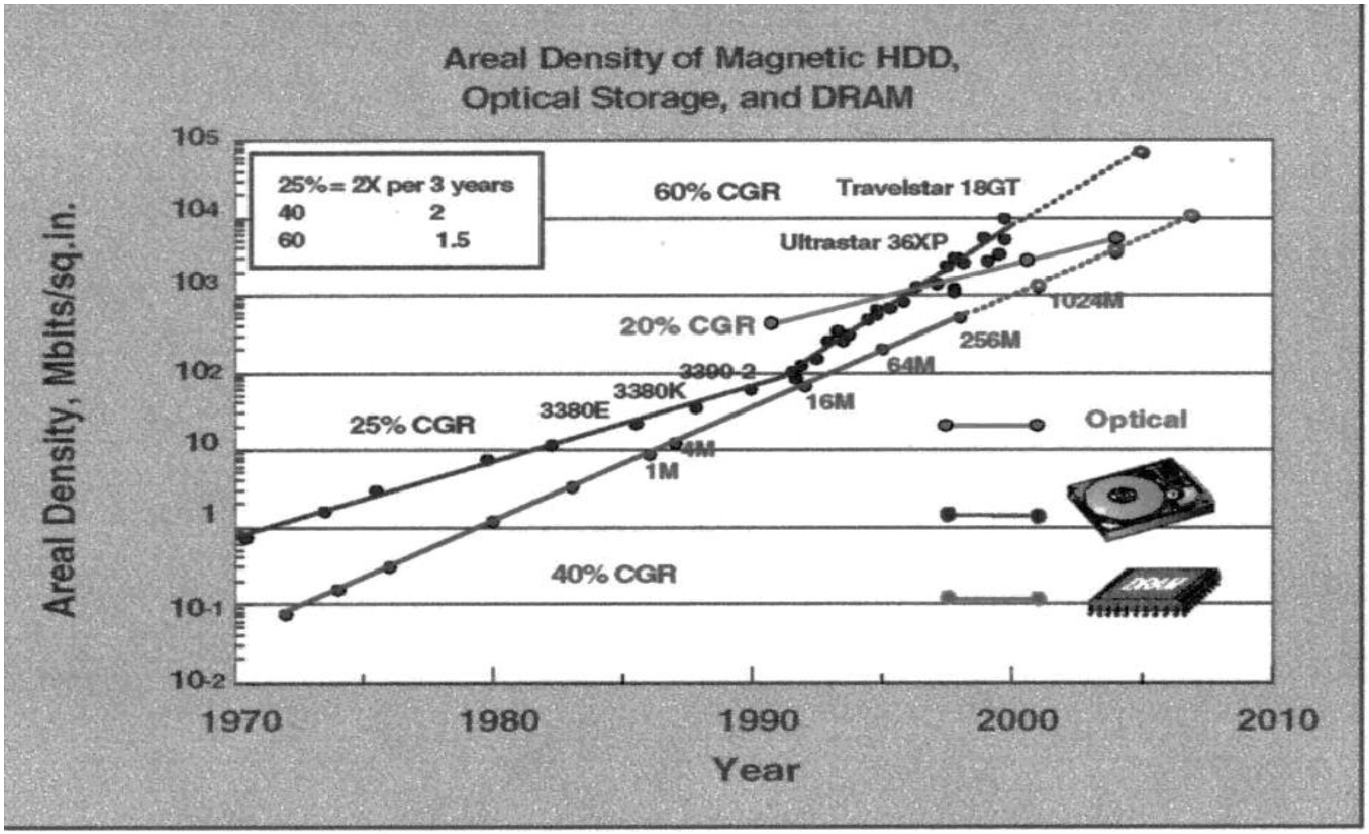
Area Density Trend (Mb/in^2 vs. Year)



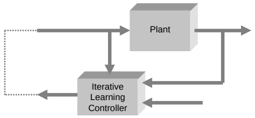
Data storage density for disk drives versus time. (Source: Ed Grochowski, IBM)



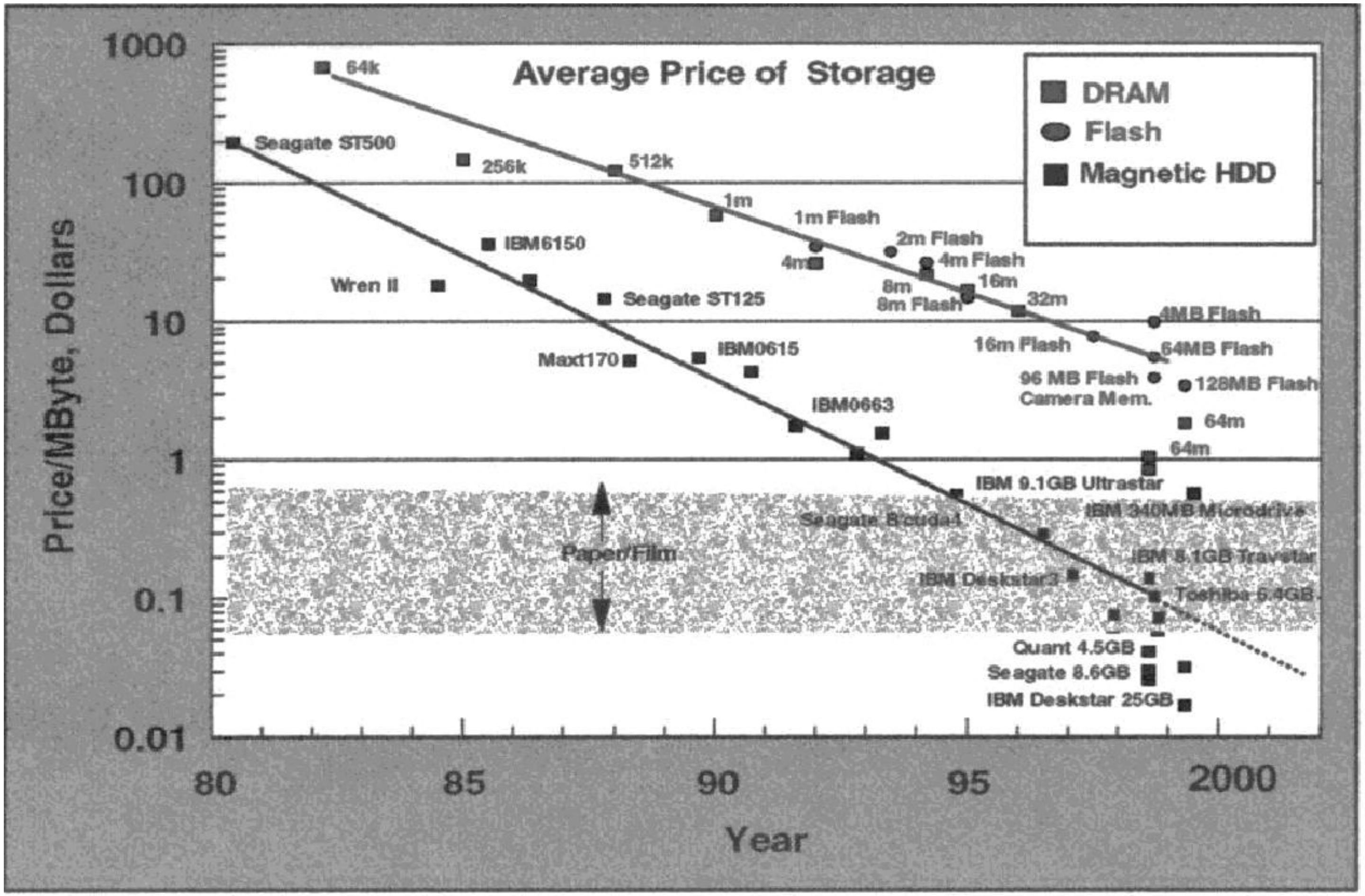
Area Density Comparison



Data storage density for magnetic disk drives, optical disk drives, and DRAM versus time. (Source: Ed Grochowski, IBM)

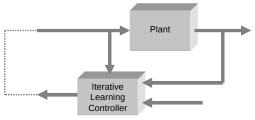


Cost Trend

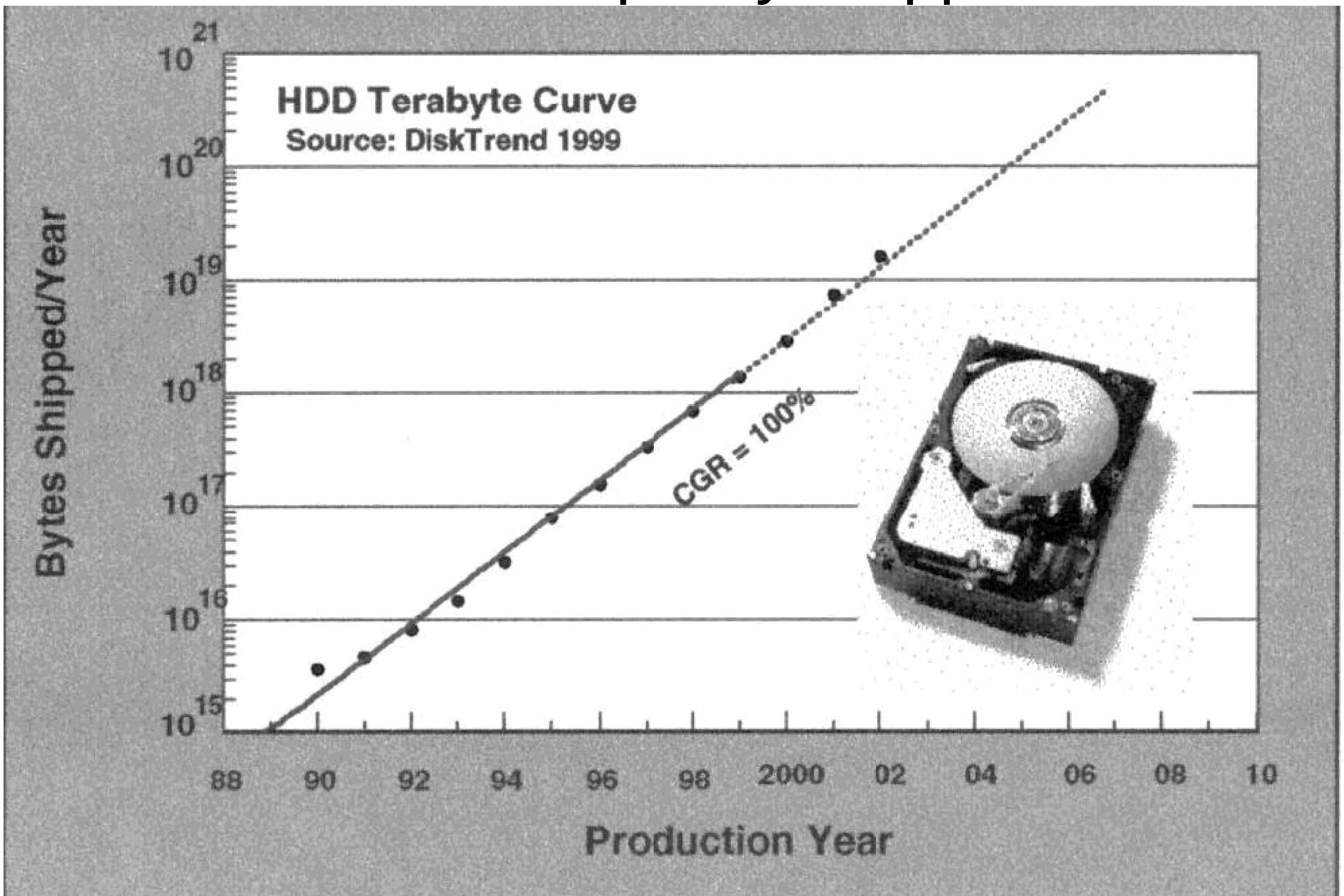


source: Ed Grochowski, IBM

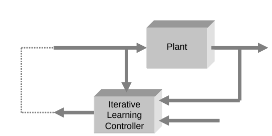
Cost of data storage for magnetic hard disk drives, DRAM, and Flash Memory



Capacity Shipped



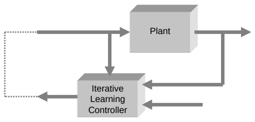
Total capacity of disk drives shipped versus time. (Source: Ed Grochowski, IBM.)



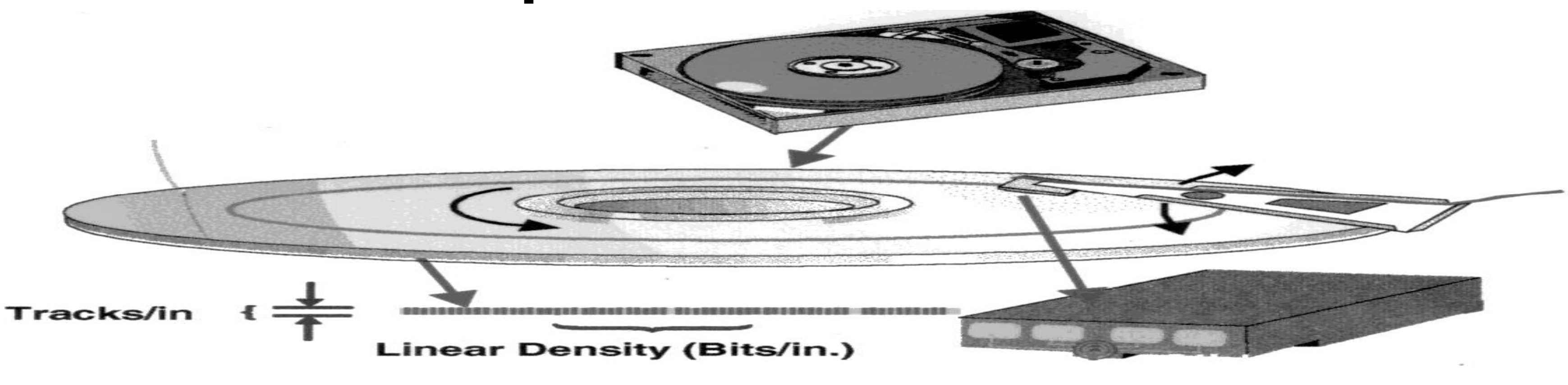
Remarks

- Cost decreases 100% yearly
- Total shipped capacity increases 100% yearly
- So, the revenue for the industry is actually flat.

- Therefore, HDD companies are extremely cost conscious! Technological innovation and lean manufacturing are equally important. For example, in Seagate, every Sr. Engineer and above must be trained (80 hours in 5-star hotel) and certified as Six-Sigma Green Belt.



Bit-Aspect-Ratio = BPI / TPI



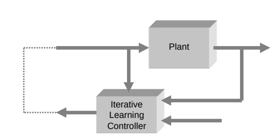
Schematic of important disk drive components. (Source: Tom Albrecht, IBM.)

•BPI (linear density) limited by the *superparamagnetic effect*. Smallest allowable magnetic grain in the media.

•If the grain smaller than critical size (10 to 12 nm. in diameter), random thermal effects will cause the grains to de-magnetize in tens of nano sec. HDD will be **volatile**, not nonvolatile for tens of years!

•So, increasing TPI (radial density), or track density, is preferred.

•High TPI solution – high capacity HDDs towards 1 $US/Gb (dream?)



- High TPI causes **TMR (track mis-registration).**

Track 10

Track 9

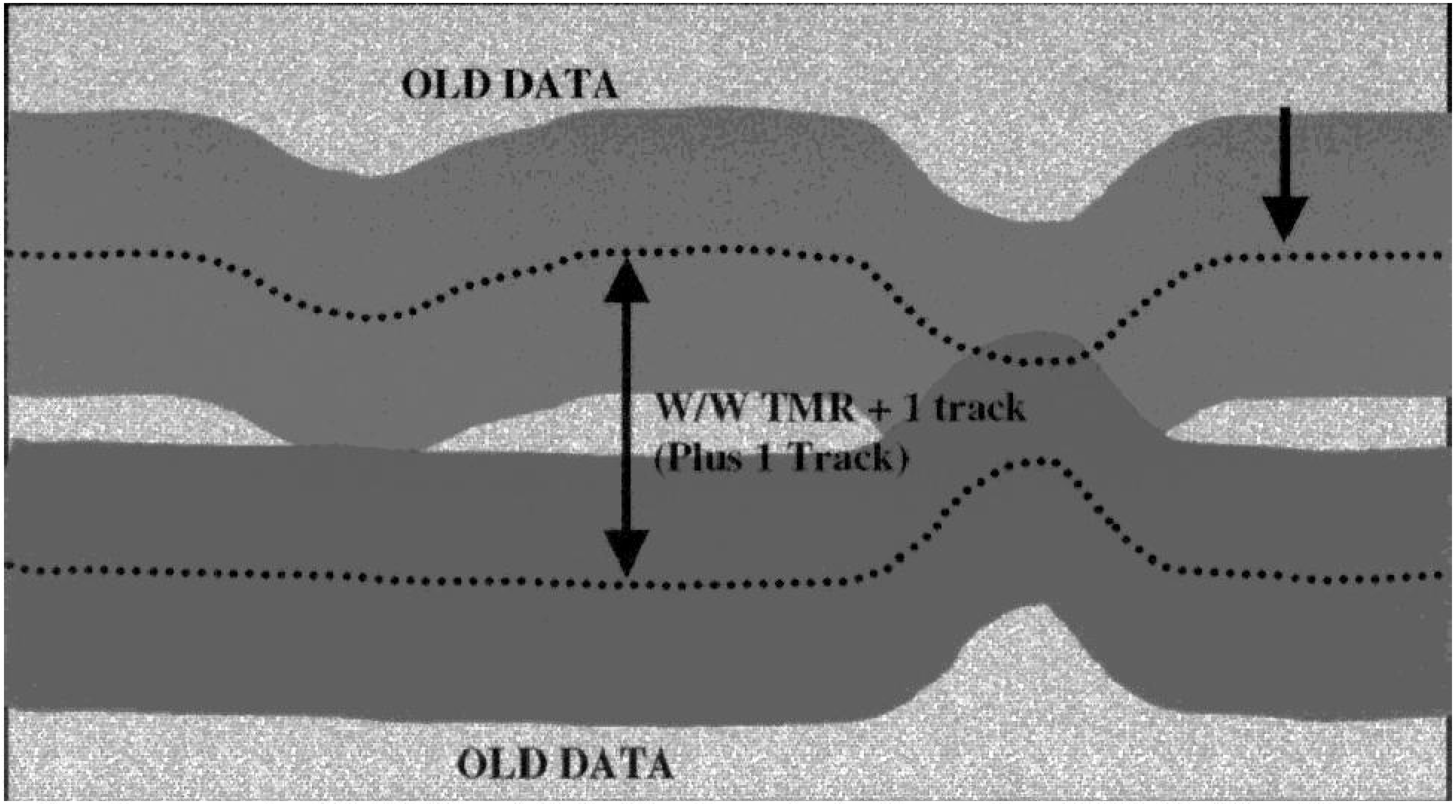


Illustration of write-to-write TMR(Track Mis-Registration). Excessive WW TMR will cause overlap between adjacent tracks, resulting recording and/or reading errors

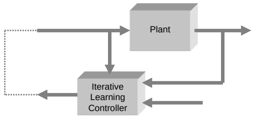
TMR : WW_TMR

High TPI challenge

Challenges

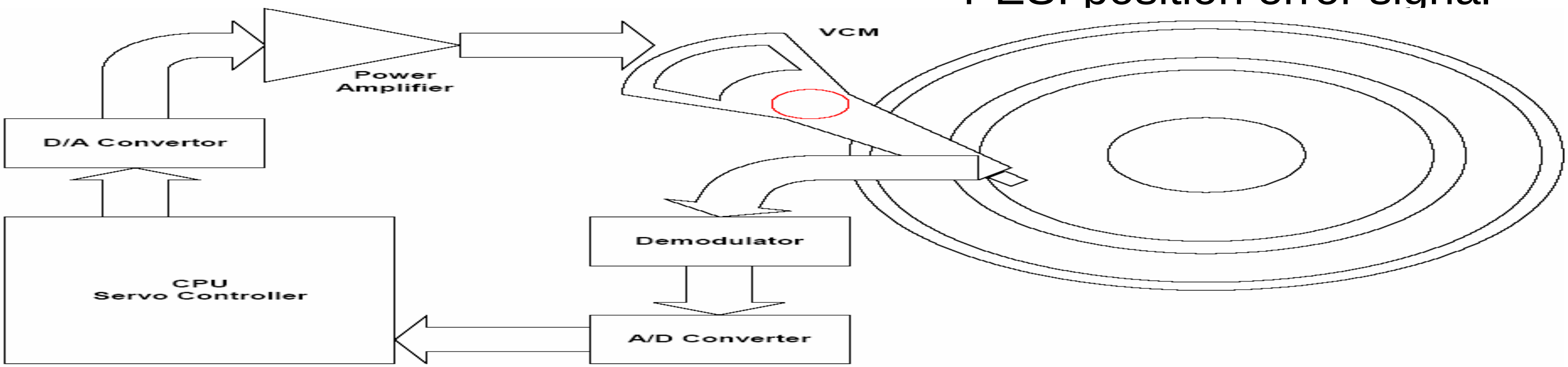
- Increasing BPI challenges head/media engineers
- Increasing TPI challenges servo/mechanical engineers with two tasks:
  - Seek: moving the head from one data track to another as fast as possible;
  - Track following: maintaining the head accurately over the data track for reading and writing operations.

- Key issues:
  - high-accuracy of track following (10% of track pitch) for good TMR budget;
  - Seek as fast as possible with less excited noise, for performance index.

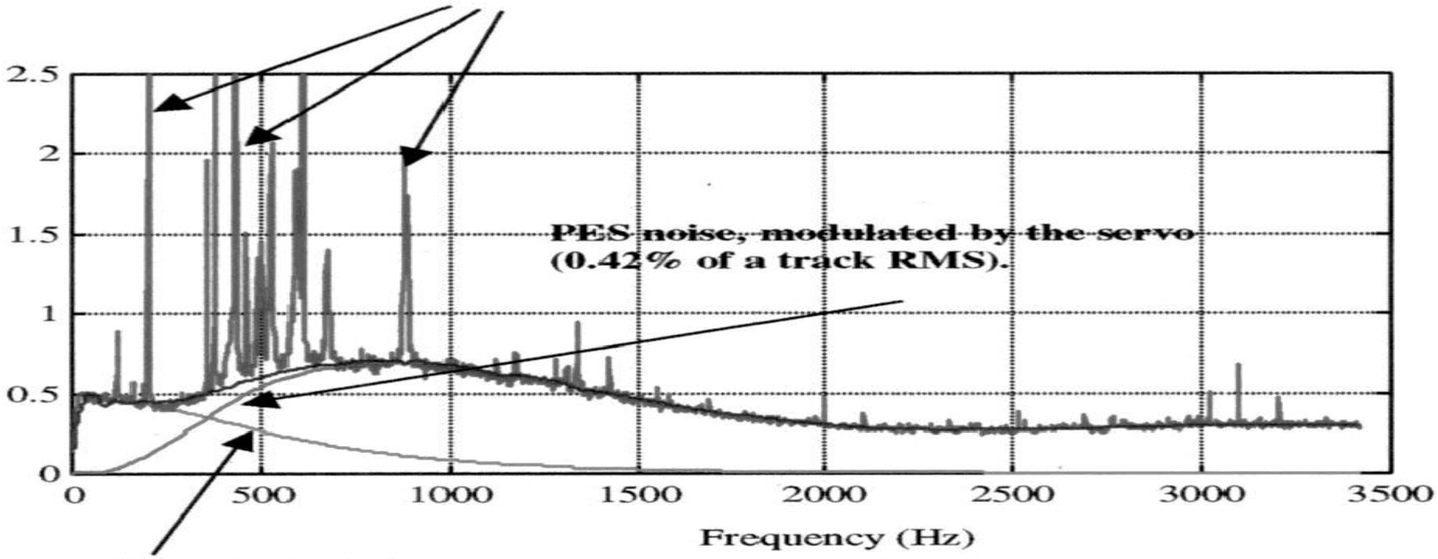


Part 3: ILC Applications

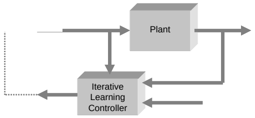
PES: position error signal



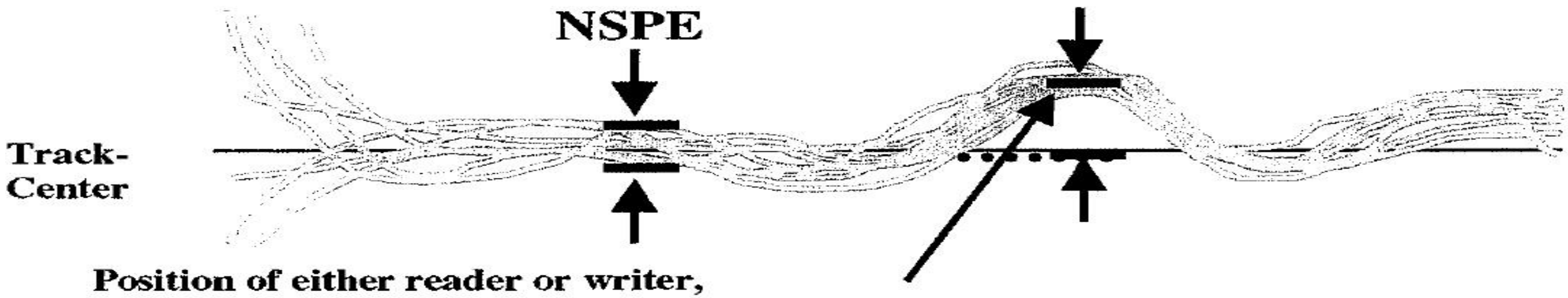
Disk vibration/spindle runout, modulated by the servo (0.33% of a track RMS).



Torques from air-turbulence, modulated by the servo (0.17% of a track RMS).

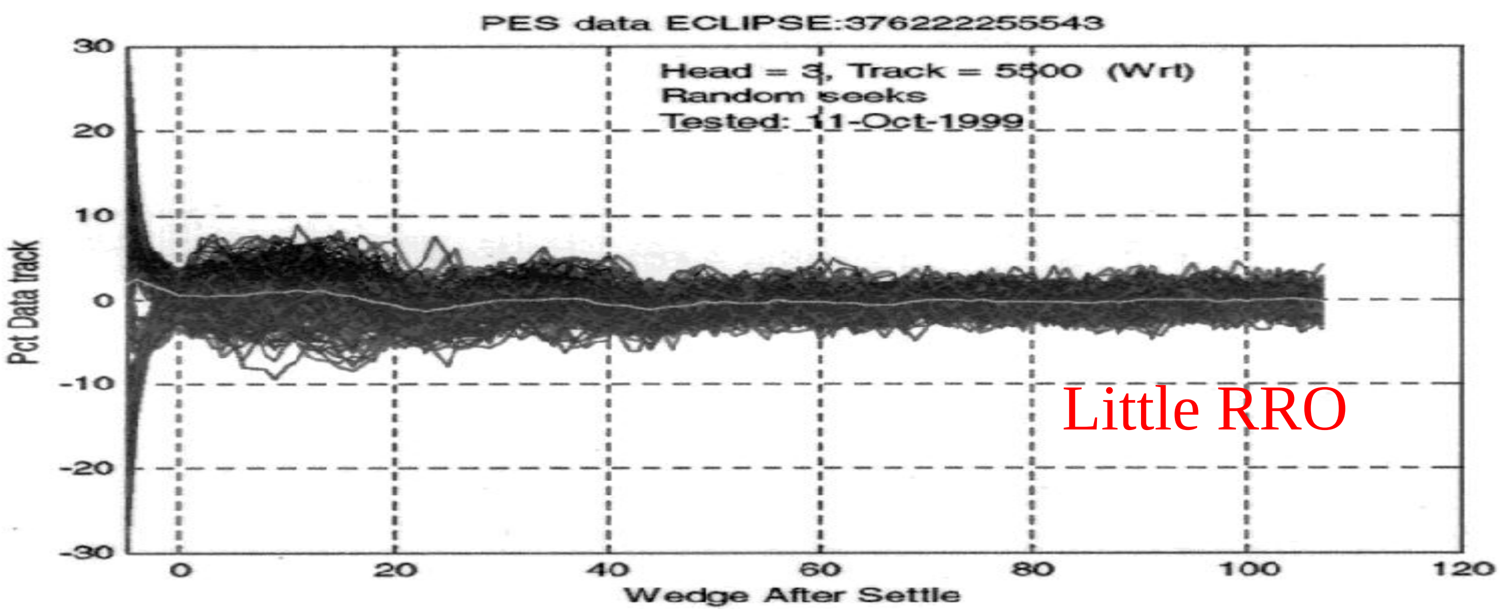


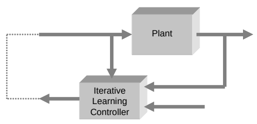
RRO vs. NRRO



Position of either reader or writer, while sitting on-track for a long time

Illustration of non-synchronous position error (NSPE) and synchronous position error (SPE).



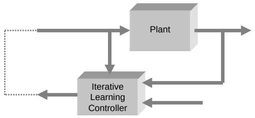


Summary: Sources of errors

- **NRRO (non-repeatable runout)**
  - PES generation noise (demodulation noise)
  - Disk vibrations
  - Actuator arm vibrations
  - Disk enclosure vibrations
  - Air turbulence (windage)
- **RRO (repeatable runout)**
  - Servo track writer (STW) error (formatting errors, noncircular eccentric tracks)
  - Sync. Vibrations (spindle motor imperfection)
- **Seek-settling**
  - Arrival errors, resonance, bias-force errors (due to friction etc.)
- Shock/vibration sensitivity

High TPI Servo Control Challenges

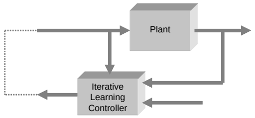
- Optimize servo / mechanics to minimize effects of errors
  - Use high loop bandwidth
    - Good mechanics
    - Dual-stage servo
  - “Clever” control schemes.
    - I will show you some soon.



Story of U6 - Seagate U Series 6 HDD Review

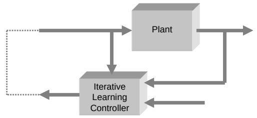
http://www.xbitlabs.com/storage/seagate-u6/

- "…the new submarine from Seagate…"
- "... today's hero - Seagate U6 drive."
- "This hard disk drive is especially interesting since it features the platters with *the highest capacity available today*: 40GB" (Two platters = 80GB. 20GB per surface.)
- "Not so long ago we had a perfect chance to see that even the drives with the activated *Automatic Acoustic Management* or AAM (i.e. those switched to a special mode when the heads are positioned slower in order to reduce the noise level) didn't perform much slower in WinBench99 than in case AAM was disabled."
- "…Seagate engineers manage to *squeeze higher performance out of these 40GB platters without increasing the prices dramatically*, Seagate will launch another drive. Then there will be another step, and the next one… Anyway, happy sailing, U6!"

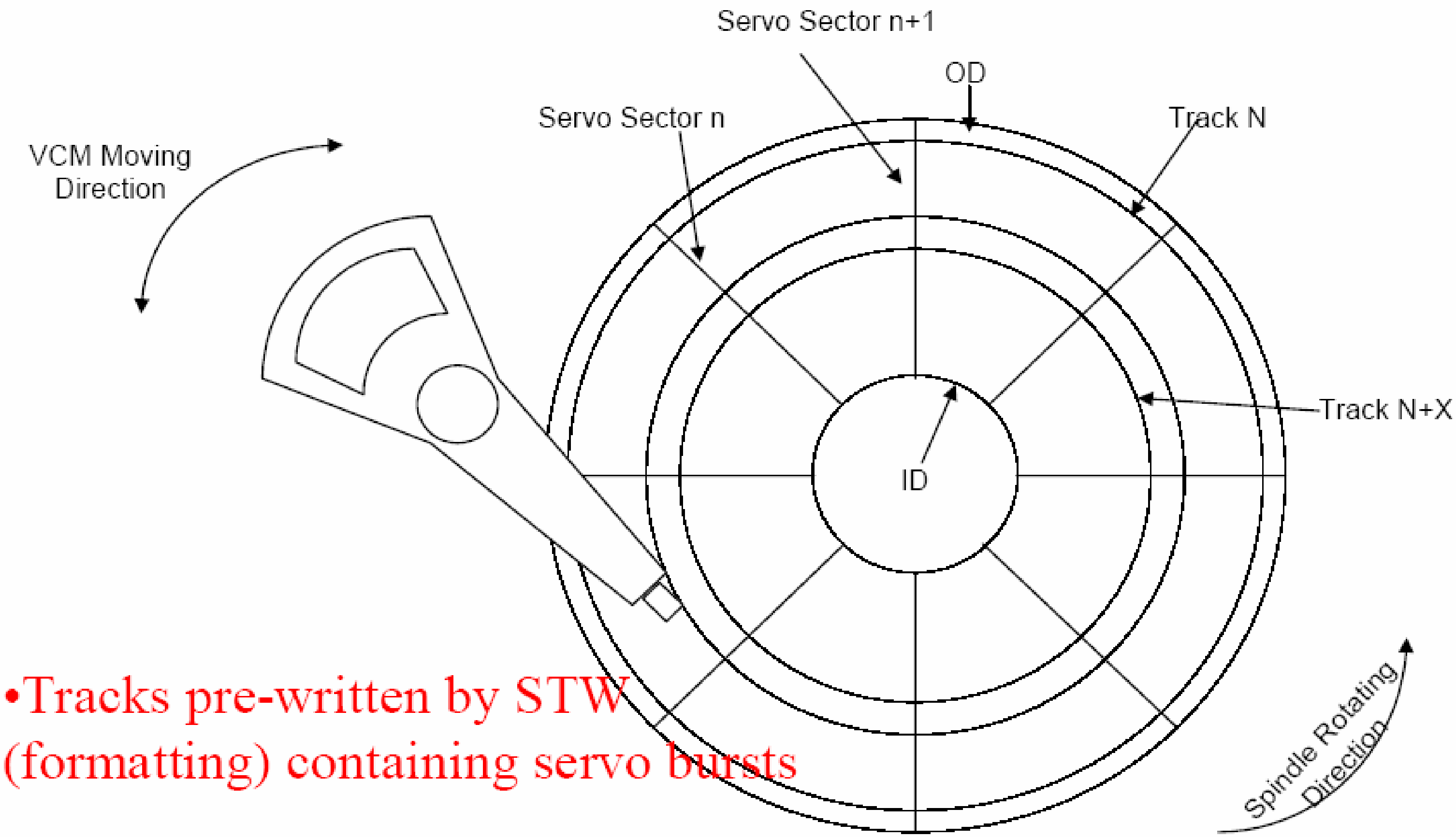


U6 Density

- W. Messner and R. Ehrlich. "*A Tutorial on Controls for Disk Drives*". **Proc. of the American Control Conference**, Arlington, VA, June 2001, pp.408-420
  - **Current highest track density 1500 tracks/mm = 38,100 TPI (BPI: 304.8 K)**
- U6 TPI: **58,000 TPI** **(BPI: >400 K)**
  - track pitch= 25.4 mm/58,000 = 497 nano
  - tracking accuracy: +/- 10% * 497 < 50 nano.
  - Note, for all HDDs, there is no conventional
    - **position sensor**
    - **velocity sensor**
    - **acceleration sensor**



Embedded Servo

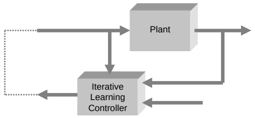


- Tracks pre-written by STW (formatting) containing servo bursts

U6 Servo Sectors = 288; Spindle 90Hz (5,400 RPM); Sampling Freq. 288*90 ~ 26 KHz

My Patents at Seagate

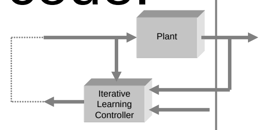
- Submitted 16 patent disclosures. All evaluated as “**pursue**” by the Patent Review Committee (**PRC**). (1999.3-2000.9)
- 3 granted US Patents 6,324,890, 6,437,936, 6,563,663. 9 pending (applications published). www.uspto.gov
- All implemented on actual hard disk drives in assembly language (Siemens C166, *16 bits/fixed-point*) in Seagate Singapore Science Park Design Centre.
- Some used in Seagate products like U8/U10 (15/30Gb) and U6 (40/80G).
- Some taken as “*trade secret*” or “*technological inventory*”.
- Received ~US$xxxyyyzzz patent awards in 2000.



Frequently Heard Dialogues

at Seagate Singapore Science Park Design Centre

- "Better?"
- "What's the price to pay?"
- "Show me on the scope (before and after)."
- "Walk me through the code."
- "Summarize up and send to (technical report) database."
- "Good new solution! Let's write a patent disclosure now!"
- "Sorry, we need poor-man's solution. Your (control) scheme is good but it's too luxurious." (26KHz -> 38 microsec.)
- "Double check the GM/PM. (gain margin/phase margin)"
- "Too busy to write a user's manual. Everything is in the code."



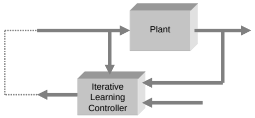
My Seagate Patents Related to ILC

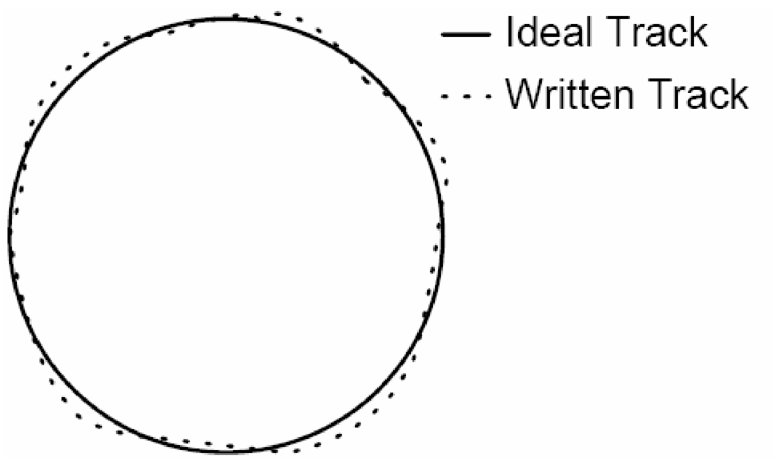
- SP-ZAP: scheduled parameter - zero-acceleration path
  - Making the track more straight to improve TMR and in turn, to increase TPI (squeeze more tracks safely)
  - US06,563,663 *Repeatable runout compensation using iterative learning control in a disc storage system*
  - US06,437,936 *Repeatable runout compensation using a learning algorithm with scheduled parameters*

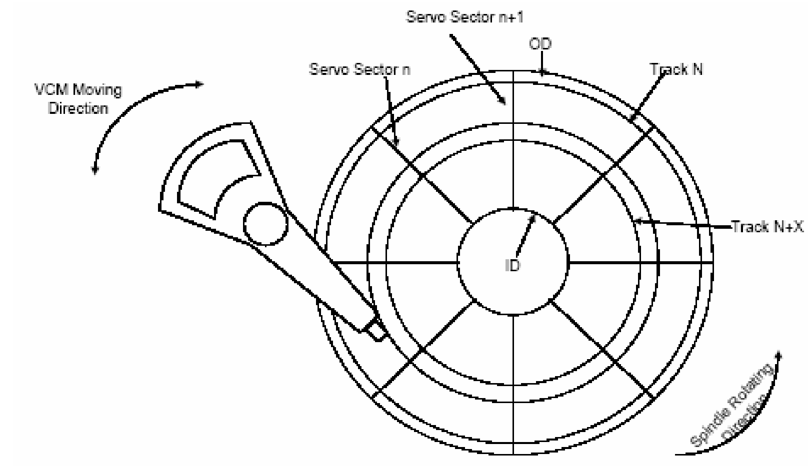
(1) Why important?

(2) How (idea)?

(3) Illustrative Drive Level Result.

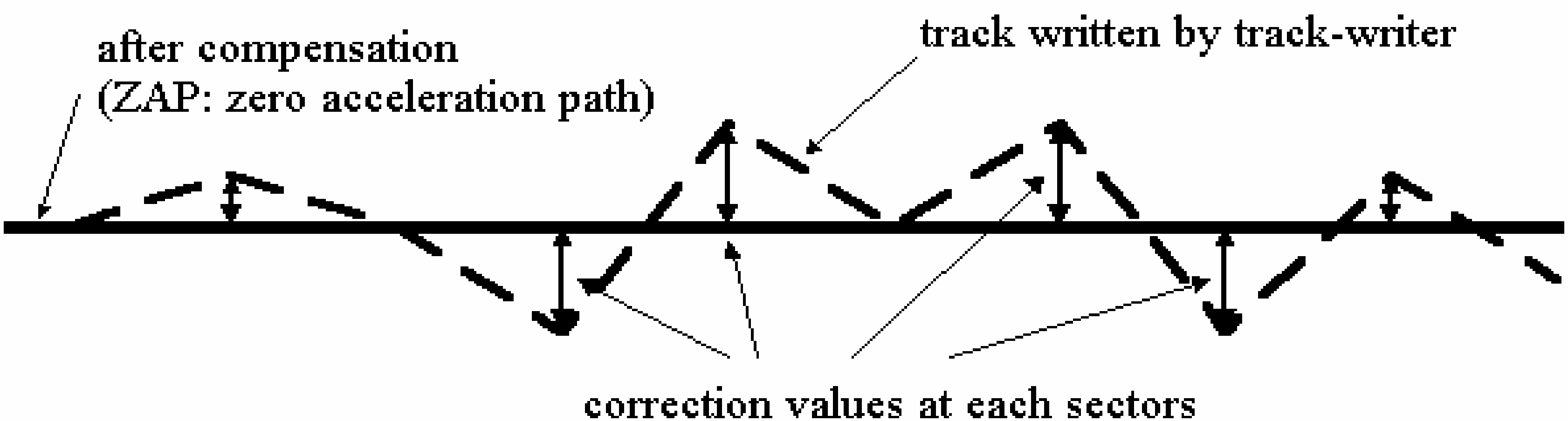






SP-ZAP Motivation

Track density is thus limited!



New Framework: Iterative Learning Control

- ZAP table: a curve deterministic (profile)
- curve identification;

optimal control problem.

- Iterative solution - ILC: *iterative learning control.*

<u>ILC concept:</u>

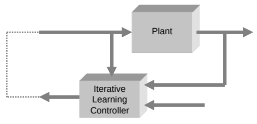
A feedforward technique.

Learning updating law:

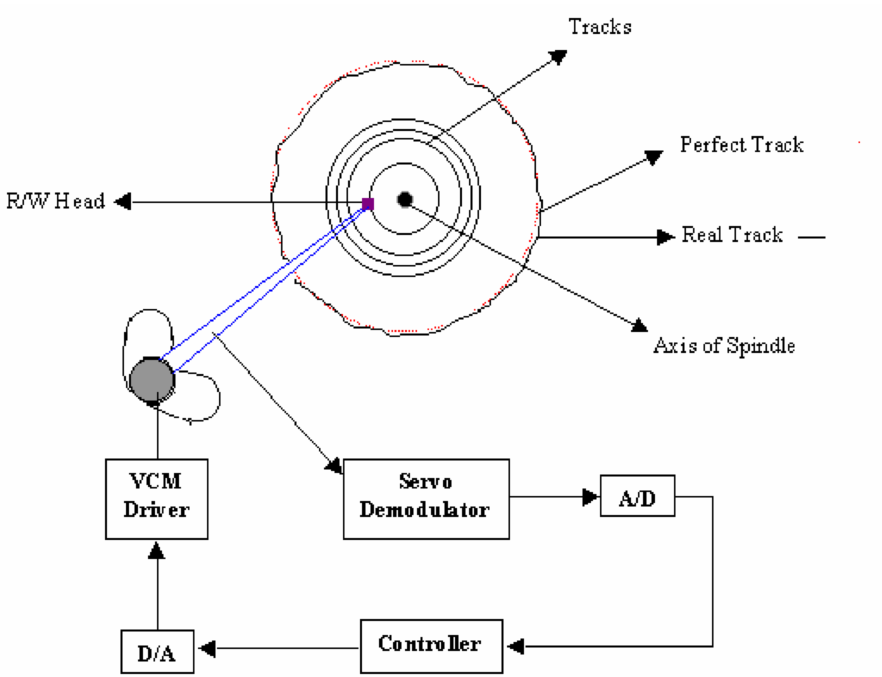
Current effort =

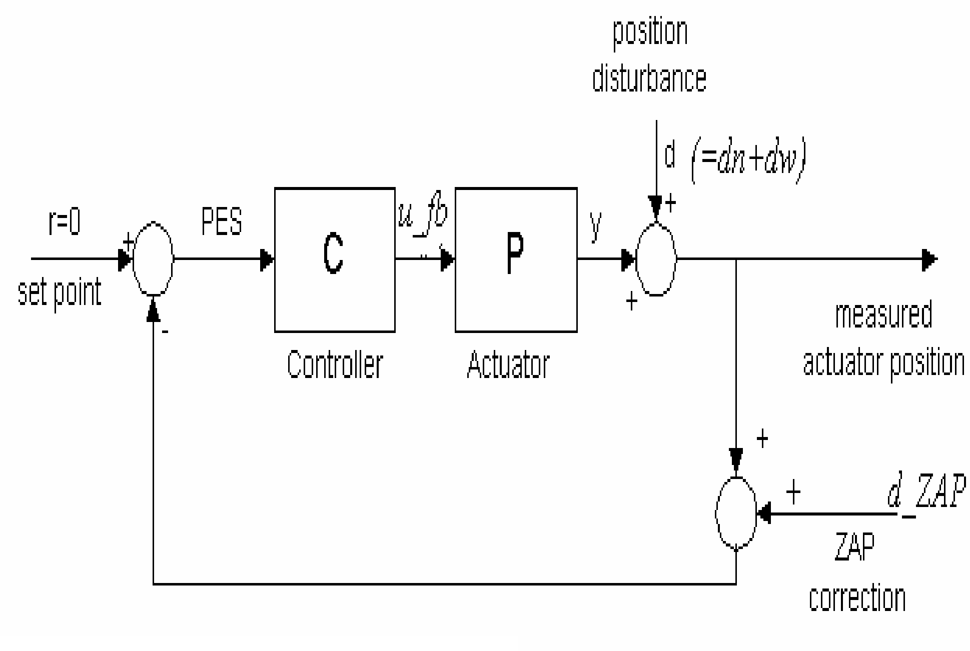
Previous effort(s)

+ Correction.



Our Servo Solution

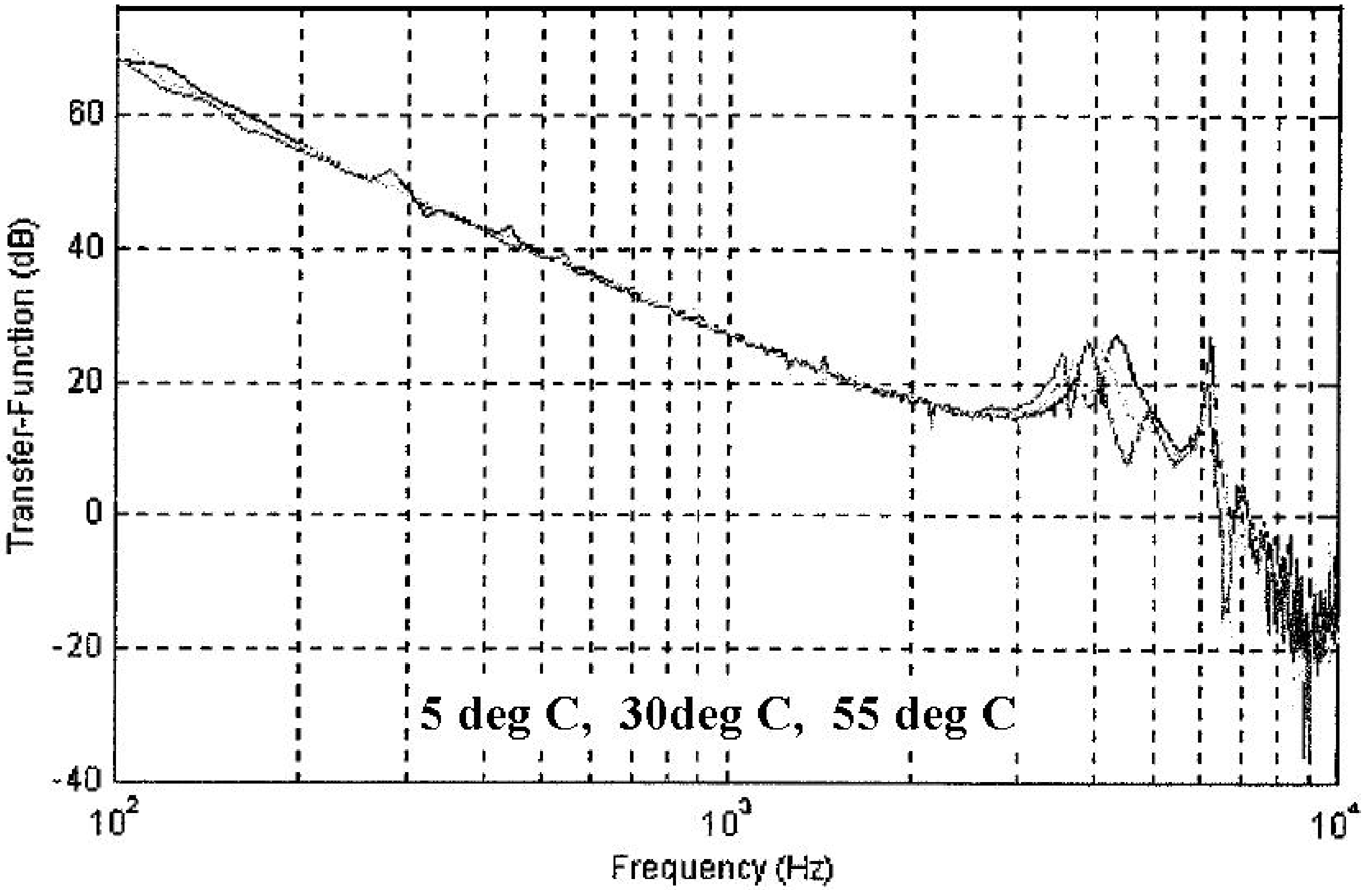




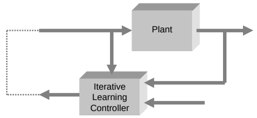
$$PES^{k} = \frac{1}{1 + P(s)C(z)}\left[r - d_{n}^{k} - d_{w} - d_{ZAP}^{k}\right]$$

- P(s) is uncertain; Only PES is measurable.

Uncertain plant Bode plots



Bode plot of the freq. response of an actuator from current input to head position output for three different ambient temperatures.



Ideal Learning Operator $\ell(\bullet)$

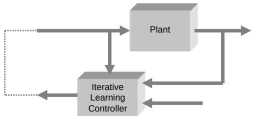
- General Learning Updating Law:

$$d_{ZAP}^{k+1}(t) = \ell(d_{ZAP}^{k}(t), PES^{k}(t), u_{fb}^{k}(t))$$

- Simple form:

$$d_{ZAP}^{k+1}(t) = d_{ZAP}^{k}(t) + \ell(PES^{k}(t))$$

- What is the ideal form for $\ell(\bullet)$??



(cont.) Ideal Learning Operator $\ell(\bullet)$

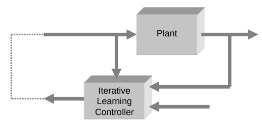
- Iterating

$$PES^{k+1} = \frac{1}{1+P(s)C(z)}[r - d_n^{k+1} - d_w - d_{ZAP}^k(t) - \ell(PES^k(t))]$$

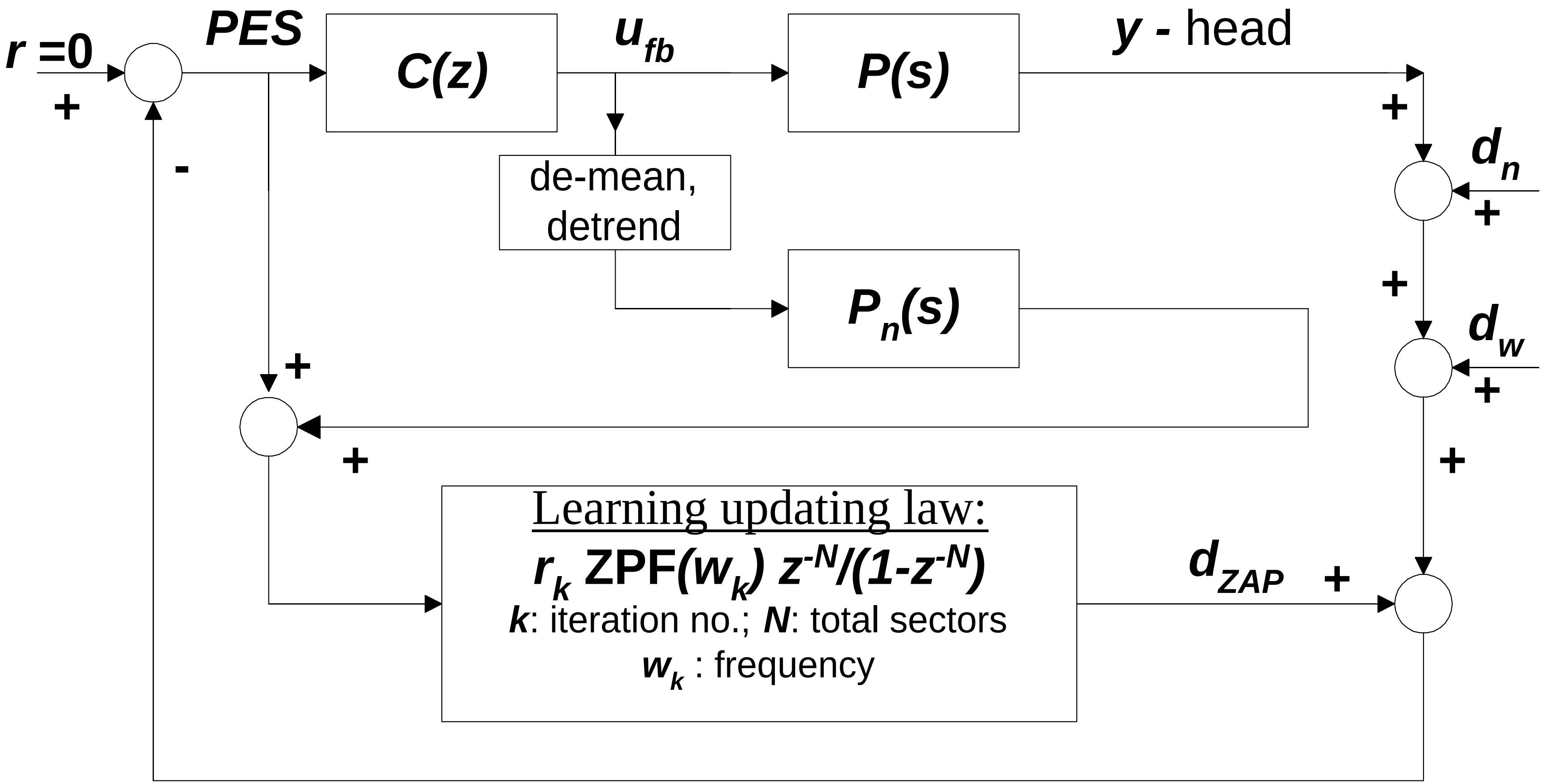
$$= (1 - \frac{\ell}{1+PC})PES^k - \frac{1}{1+PC}(d_n^{k+1} - d_n^k).$$

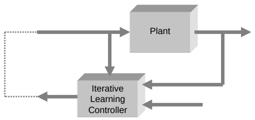
Learning rate: $\rho(\omega) = 1 - \frac{\ell}{1+PC}(j\omega)$

Ideal learning operator : $\ell(j\omega) = 1 + P(s)C(z), \ \forall\omega$



Our Solution in block diagram





Our solution in equations.

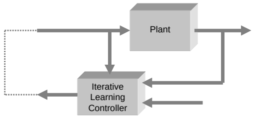
- SP-ZAP learning updating law

$$d_{ZAP}^{k+1}(t) = d_{ZAP}^{k}(t) + r_k ZPF(\omega_k, z, z^{-1})[PES_k + P_n(s)u_{fb}]$$

P_n : *nominal VCM model* ***(just a double integrator)***

- Learning operator:

$$\ell(\bullet) = r_k ZPF(\omega_k, z, z^{-1})[1 + P_n(s)C(z)]$$



Learning Convergence analysis

<u>PES Learning Convergence</u> :

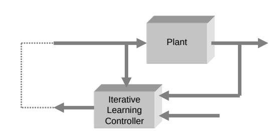
$$PES^{k+1} < \rho^{k+1}(\omega) PES^{0} - \frac{1-\rho^{k+1}(\omega)}{1-\rho(\omega)} \frac{1}{1+PC} \hat{d}_n$$

<u>Learning Convergence condition</u> :

$$\rho_\omega = |\rho(\omega)| = \left| 1 - \frac{\ell}{1+PC}(j\omega) \right| < 1, \quad \forall \omega < \omega_s / 2$$

<u>ZAP-table Learning Convergence</u> :

$$d_{ZAP}^{k+1} = \rho^{k+1}(\omega) d_{ZAP}^{0} - (1-\rho(\omega)) \sum_{j=0}^{k} \rho^{j}(\omega) d_n^{k-j} - (1-\rho^{k+1}(\omega)) d_w \approx -d_w$$



SP: Scheduling Parameters

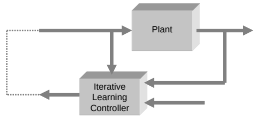
- Learning gain
- Cutoff frequency of the zero phase filter (ZPF)
- Phase advance
- Servo loop gain

<u>OBJECTIVES of SP:</u>

robustify learning process;

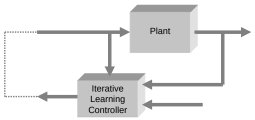
improve learning performance

reduce the learning cost (parsimoniousness)



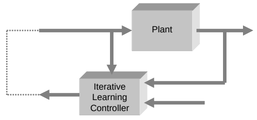
Benefits of SP-ZAP Algorithm

- Scheduling Parameters:
  - Learning gain
  - Cutoff frequency of the zero phase filter (ZPF)
  - Phase advance
  - Servo loop gain
- Benefits:
  - Iteration Used
  - Robustifying learning process;
  - Improved learning performance;
  - Simple. Cheap. No FFT/IFFT



U8 ZAP Algorithm Summary:

- 1. Lower the servo loop gain and then collect 3 revs *PES* and *Udac*. Do averaging. Get *PES_a* and *Udac_a*
- 2. Demean *Udac_a* and then double integrate it. Get *Udac_II*
- *3. ZAP_table_1=(PES_a*+Klump**Udac_II)*Learning_Gain_1*
- *4. ZPF for the first ZAP_table_1* (NOTE: *ZAP_table_0*=0)
- *5. Repeat 1 with an increased servo-loop gain.*
- *6. Repeat 2*
- *7. ZAP_table_2=ZAP_table_1+*
  (PES_a+Klump**Udac_II)*Learning_Gain_2*
- *8.* Set servo-loop gain to normal.
- *SP-ZAP finished with total 6 revs and 2 iterations..*



Results on U8 (2): Average Performance

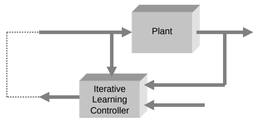
– Average over tracks from OD to ID.

– HDD information: U8, SP4, 4H, GP A2, serial # 3CV00006

– Code information: U8 – ST34313A 01.01.021 SRVO ROM: Atlantis3-40MHz P, Giorgione, GC80, SrvoDebug, SrvoMode, Digital Burst,EM2.

– Case-1: 16R4I **: four iterations, each iteration collecting four revs data for averaging.**

– Case-2: 6R2I : **two iterations, each iteration collecting three revs data for averaging.** This is the scheme we shall use in U8**.**



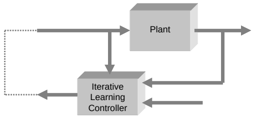
Results on U8 (2): Average Performance

Table 1. Averaged WI-RRO learning performance for **Case-1.**

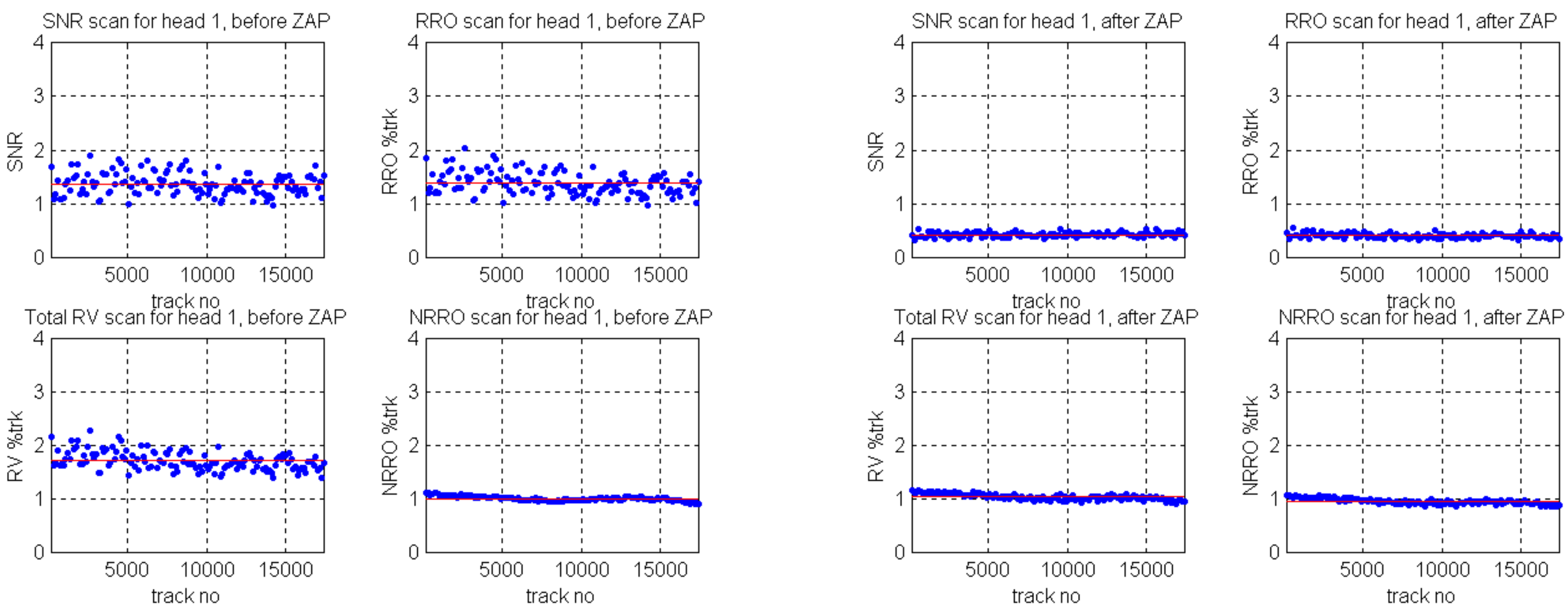
Head #	η_{RRO} %	η_{NRRO}	η_{RV} %	notes
1	70.01	5.1	**38.9**	16R4I/GS/ZPF

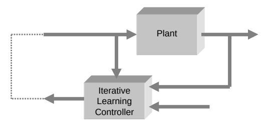
Table 2. Averaged RI-RRO learning performance for **Case-2.**

Head #	η_{RRO} %	η_{NRRO}	η_{RV} %	notes
1	51.14	3.54	**31.26**	6R2I/GS/ZPF



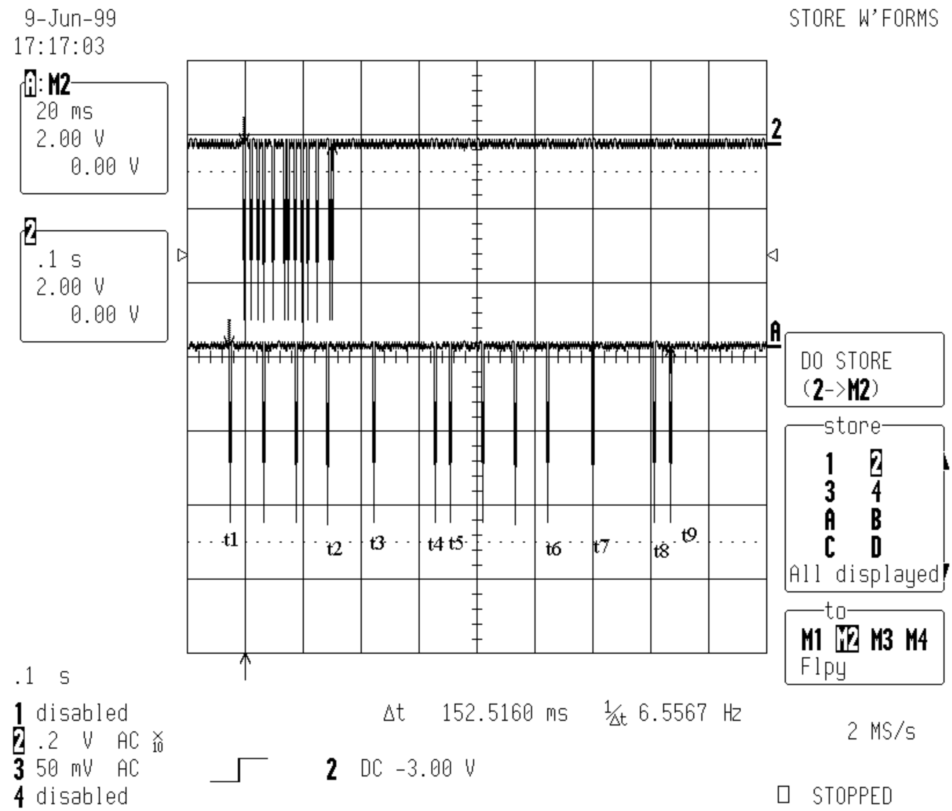
Results on U8 (2): Average Performance



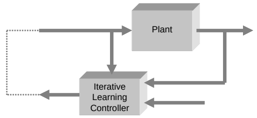


Results on U8 (3): Process Time Estimate

- t1-t2: **34.3 msec. 3 revs of PES/UDAC collection;**
- **t2-t3: 15.3 msec. averaging PES/UDAC;**
- **t3-t4: 21.7 msec. calculating;**
- **t4-t5: 4.60 msec. learning law (ZAP table) updating;**



- In total: 151.8 msec.
- 0.1518*4*18000/3600 = 3.05 hours. <u>45 min. /head.</u>
- <u>Goal:>50% RRO, >20% RO</u>

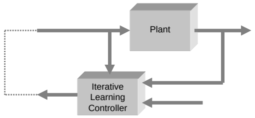


Results on U8 (4): Quantization Effect

- EF bursts provide 7-9 dibits. Quantization levels = 3 to 4
- Resolution=counts per erase pattern.

Table 3. Averaged RI-RRO learning performance for **Case-2.**

Head #	η_{RRO} %	η_{NRRO}	η_{RV} %	notes
1	51.14	3.54	**31.26**	6R2I/GS/ZPF
1	27.39	2.98	18.34	ibid, quantization level 4; resolution=*4 counts/dibit*
1	27.25	2.45	17.93	ibid, but resolution=*3 counts/dibit*
1	27.77	2.24	18.43	ibid, but resolution=*5 counts/dibit*



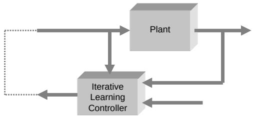
Results on U8 (5): Robustness on **Klump**

- Use 1R1I scheme.
- *Klump* +/- 20% around its nominal value.

Table 4. Averaged RI-RRO learning performanc**.**

Head #	*Klump*	η_{RRO} %	η_{NRRO}	η_{RO} %	notes
2	+20%	37.0	10.4	**21.42**	5R5R GS/ZPF
2	0	36.5	10.1	**20.97**	ibid,
2	-20%	32.2	7.6	**17.70**	ibid,
3	+20%	46.5	3.1	**22.50**	6R6R GS/ZPF
3	0	46.8	3.2	**22.53**	ibid,
3	-20%	47.4	2.62	**22.30**	ibid,

Conclusion: **SP-ZAP scheme is quite robust w.r.t.** Klump

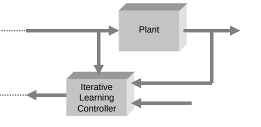


Benefits from Scheduled Parameters

- Learning gain scheduling - faster learning convergence.

Table 5. Averaged RI-RRO learning performance for **HDA-1.**

Head #	η_{RRO} %	η_{NRRO} %	η_{RO} %	notes
1	60.85	2.85	**33.81**	20R5I, learning gain 0.2 const.
1	55.50	3.69	**32.89**	8R2I, γ_1, γ_2 according to (5), with ZPF



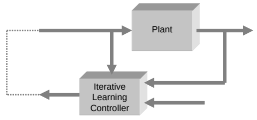
Benefits from Scheduled Parameters

- Servo loop gain scheduling - improves the learning performance. Increase the servo loop gain from a lower value than normal.

Table 6. Averaged RI-RRO learning performance for **HDA-1.**

Head #	η_{RRO} % w/ZPF	η_{RRO} % w/o ZPF	η_{NRRO} % w/ZPF	η_{NRRO} % w/o ZPF	η_{RV} % w/ZPF	η_{RV} % w/o ZPF	Notes
1	16.59	-7.92	2.73	3.18	11.81	-3.76	4R1I
1	**55.5**	**35.64**	**3.69**	**4.90**	**32.89**	**23.95**	**8R2I**
1	70.01	54.5	5.10	5.25	39.60	33.54	16R4I

Note: "Learning gain scheduling" is also used.



Benefits from Scheduled Parameters

- ZPF - safeguard the learning convergence. Learn the lower frequency contents of ZAP table first.

Table 6. Averaged RI-RRO learning performance for **HDA-1.**

Head #	η_{RRO} % w/ZPF	η_{RRO} % w/o ZPF	η_{NRRO} % w/ZPF	η_{NRRO} % w/o ZPF	η_{RV} % w/ZPF	η_{RV} % w/o ZPF	Notes
1	16.59	-7.92	2.73	3.18	11.81	-3.76	4R1I
1	**55.5**	**35.64**	**3.69**	**4.90**	**<u>32.89</u>**	**23.95**	**8R2I**
1	70.01	54.5	5.10	5.25	39.60	33.54	16R4I

Note: “Learning gain scheduling” is also used.

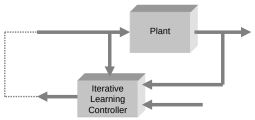
Benefits from Scheduled Parameters

Table 7b. Averaged RI-RRO learning performance for **HDA-1. Head #3**

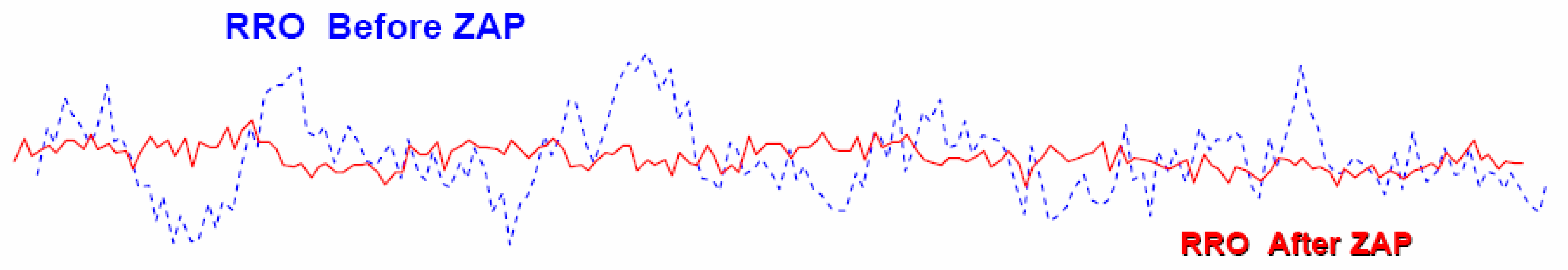
α_1 dB	α_2 dB	η_{RRO} %	η_{NRRO} %	η_{RV} %	Notes
0	0	49.68	2.50	32.66	8R2I
-3	**-2**	**55.95**	**1.85**	**35.59**	**8R2I**
-5	-3	57.24	2.79	36.62	8R2I

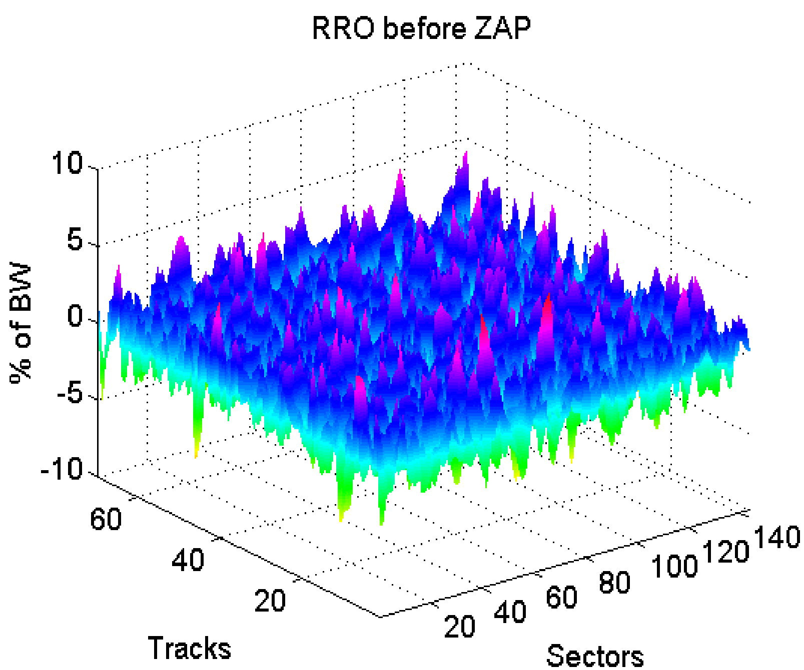
Table 8. Averaged RI-RRO learning performance for **HDA-2. Head #3**

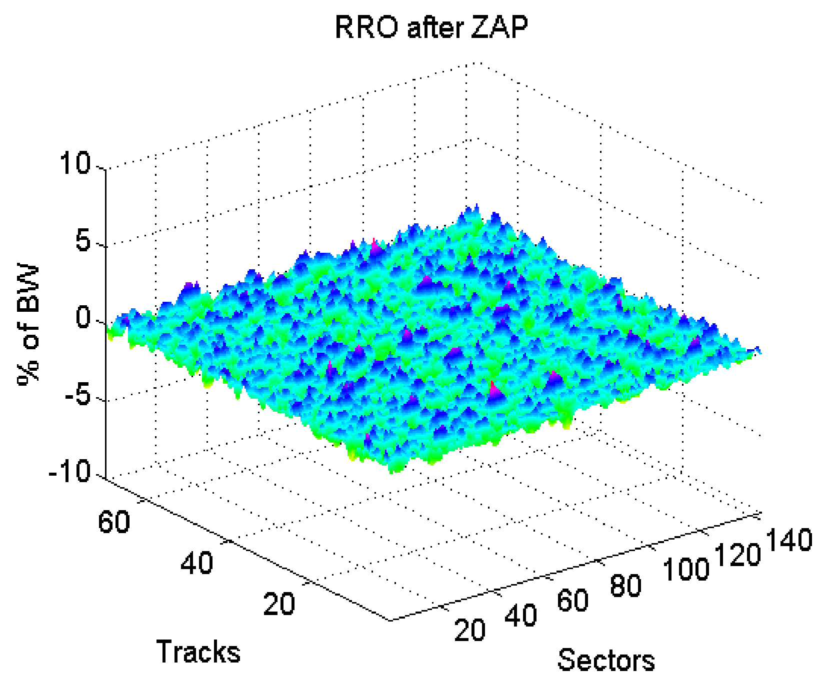
α_1 dB	α_2 dB	η_{RRO} %	η_{NRRO} %	η_{RV} %	Notes
0	0	42.86	2.27	20.5	8R2I
-3	**-2**	**46.84**	**2.70**	**22.36**	**8R2I**
-5	-3	45.16	2.54	21.16	8R2I

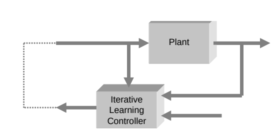


Before and After ZAP

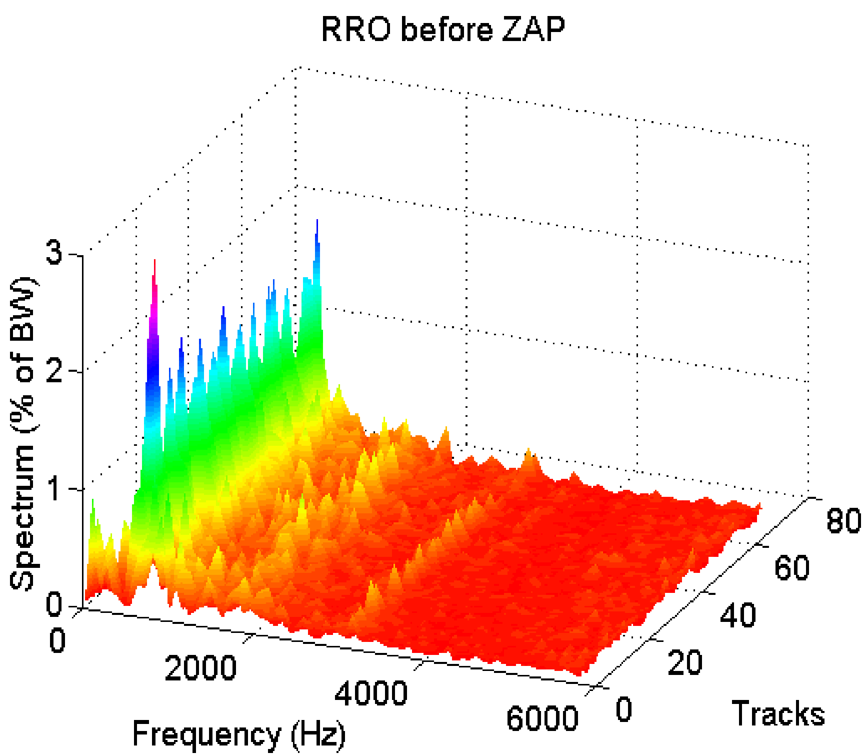


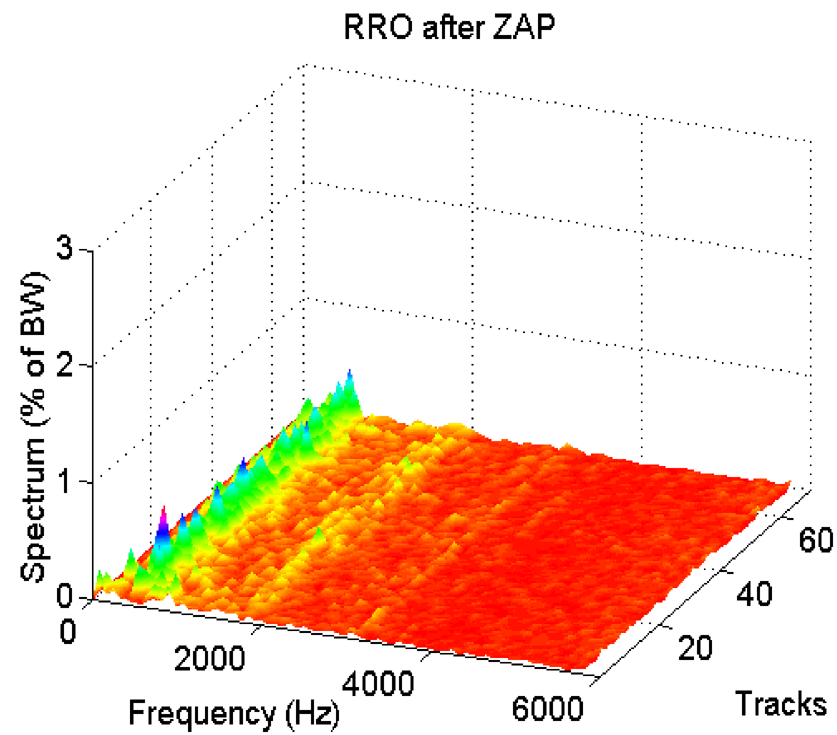


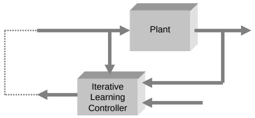




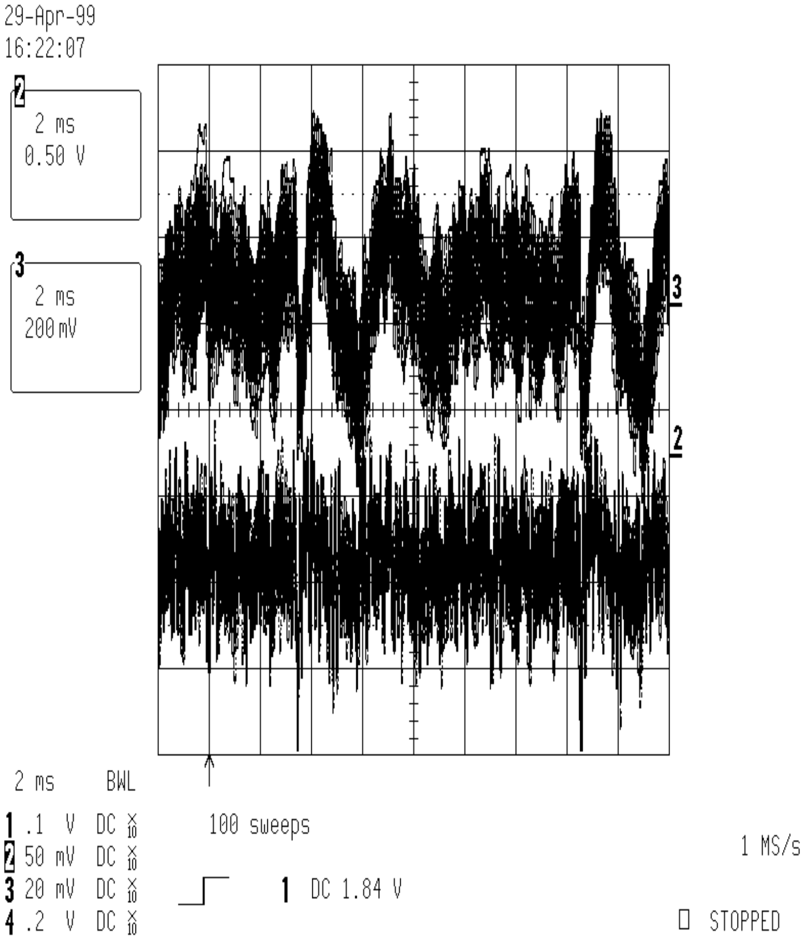
Before and After ZAP Spectrum

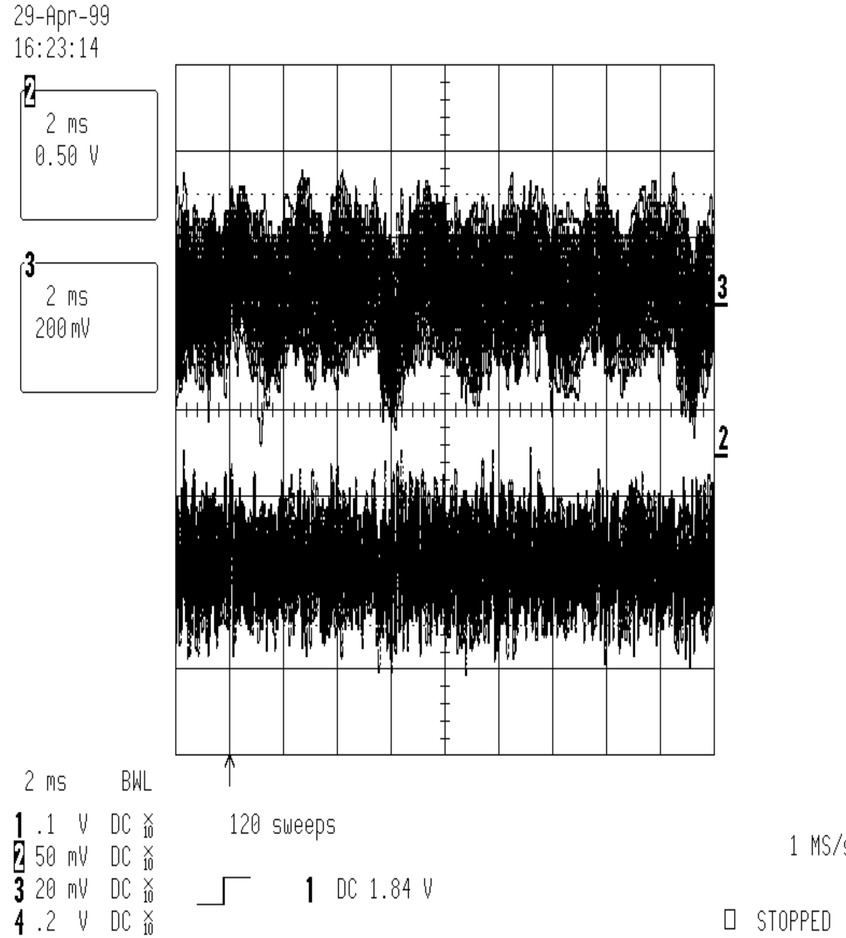




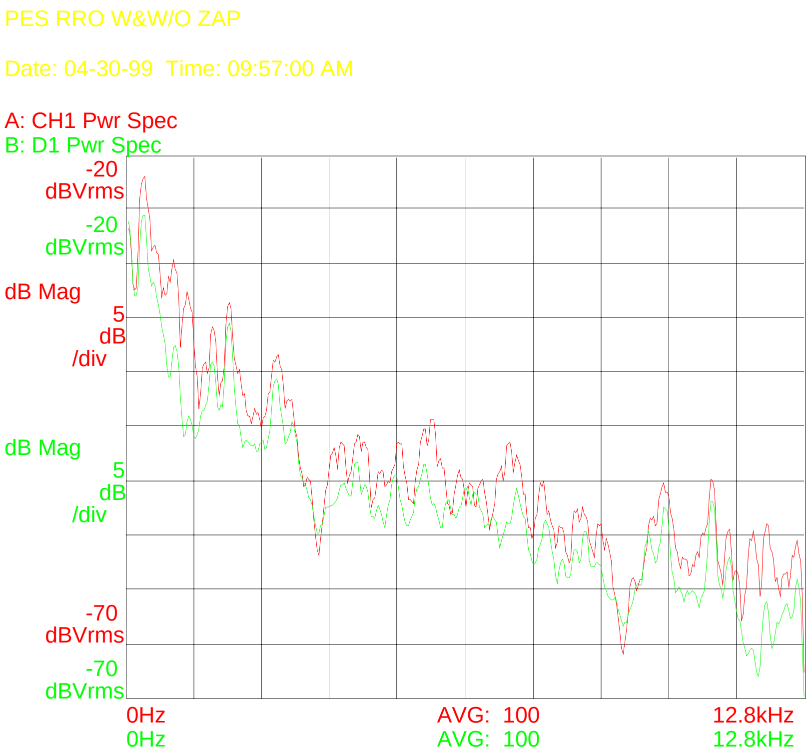


Before and After ZAP: Scope Impression

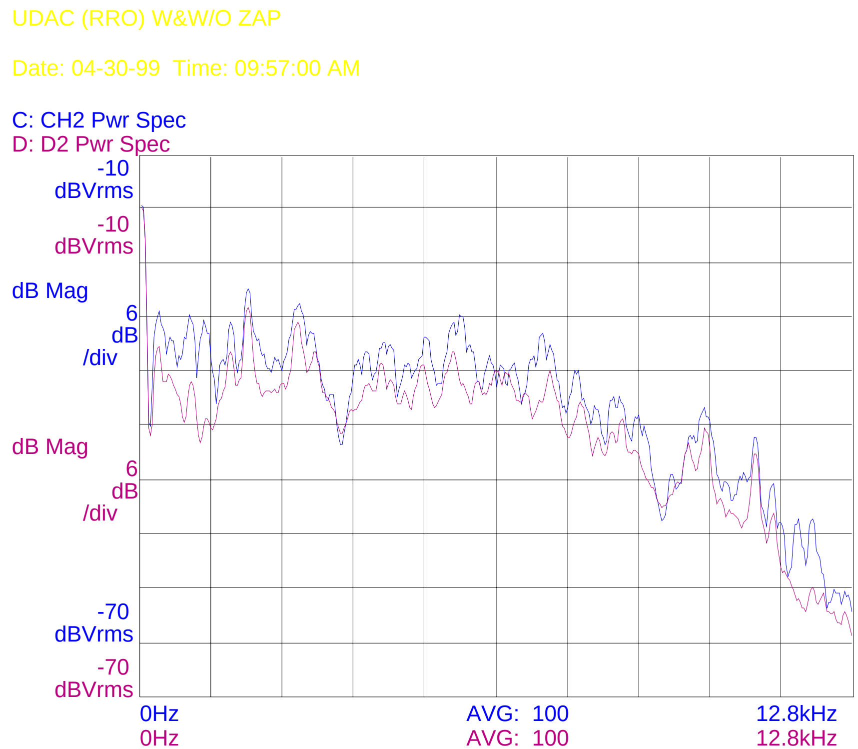




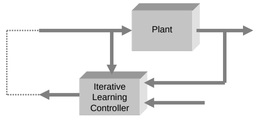
Before and After ZAP: Spectrum



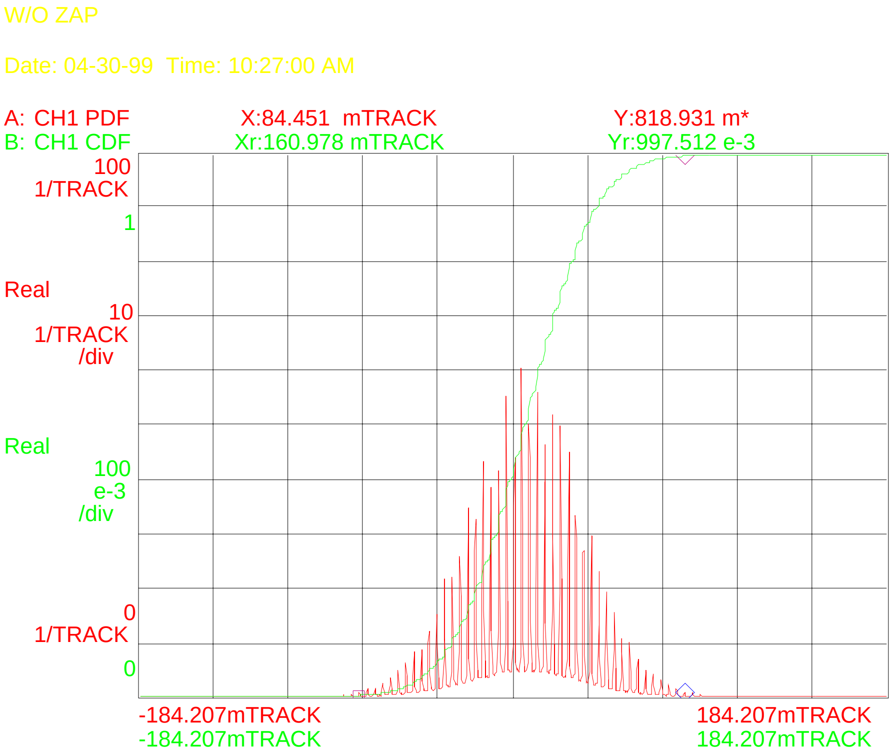
PES Spectrum: Before / After

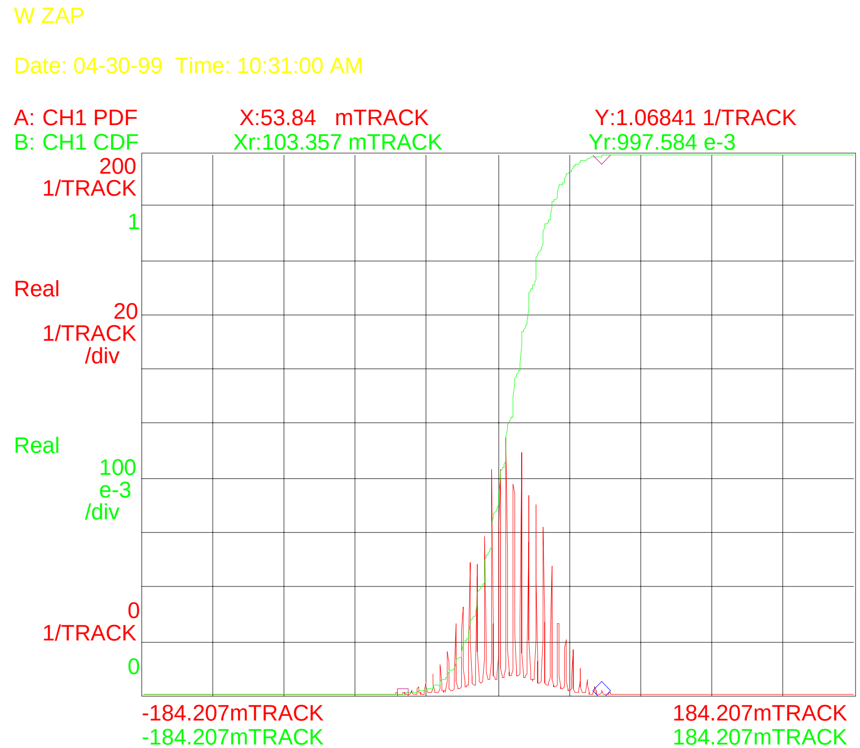


UDAC Spectrum: Before / **After**



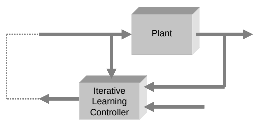
Before and After ZAP: PDF/CDF



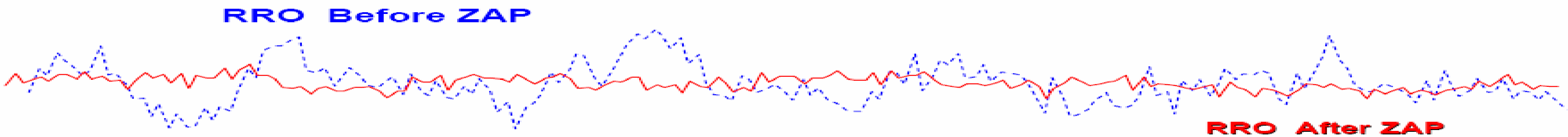


PES PDF/CDF : Before

PES PDF/CDF : After



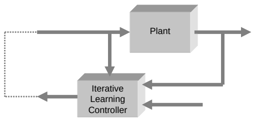
Summary of SP-ZAP



- **Benefits**
  - Increase TPI and double the HDD capacity. Or, for the same TPI, increase the reliability
  - *Purely* algorithm/code change
  - Reduce STW cost
  - Show the power of advanced control idea
  - …

- **Price to pay**
  - Extra time to learn the compensation table during factory process
  - Better servo demodulator chip to embed the learned compensation table

Used in U6 (40/80Gb) 58KTPI Production Line



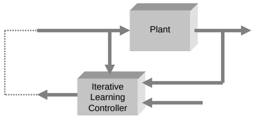
References

•**[1] Yangquan Chen and KK Ooi,** *A Zero Acceleration Path (ZAP) Compensation Algorithm Using Scheduled Parameters (SP-ZAP).* **Technical Report (draft), 06-04-99. Seagate Singapore Science Park.**

•**[2] Servo Group,** *SP-ZAP Implementation Results – Stage-1*. **Technical Report. 29-04-99. Seagate Singapore Science Park.**

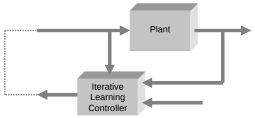
•**[3] Servo Group,** *SP-ZAP Implementation Results – Stage-2.* **Technical Report. 14-05-99. Seagate Singapore Science Park.**

•**[4] Servo Group,** *Performance Characterization of SP-ZAP for Use with U8. (SP-ZAP: WI-RRO Curve Learning Algorithm Using Scheduled Parameters To Achieve ZAP).* **Technical Report. 11-06-99. Seagate Singapore Science Park.**



Other Issues

- ZAP Table repeatability from track to track
- Remove 1F, 2F, 3F?
- ZAP table read-back error tolerance
- RRO/NRRO ratio – what if NRRO dominant?
- Learning ZAP table always from zero? Or starting from the table of adjacent track?
- Dual actuator RRO compensation?
- Servo track writer RRO ZAP?



Solution 1: Do not ZAP out fundamental component ?

- To achieve ZAPath, fundamental component in Written-In RRO needs to be ZAPed out;
- In selfservo, fundamental component in the previous track needs to be ZAPed out. (e.g., a spike in one burst, which also contribute large amplitude in fundamental component).

Solution 2: Do not ZAP out cross-track repeatable part of PES RRO

•Cross-track repeatable part of PES RRO is more than 50% of the total PES RRO

•Remove this part will result a smaller ZAP table

Solution 3: Remove the cross-track repeatable in ZAP tables

- **ZAP table amplitude will be reduced by 50%**

Remarks on Solution 2 & 3:

- **Since cross-track repeatable part of PES RRO or disturbance does not contribute to track squeeze, they need not to be ZAPed out.**
- **They will not increase track squeeze comparing with normal ZAP**